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THE DESIGN, DEVELOPMENT AND EVALUATION OF IMPROVED STC EQUIPMENT FOR APPLICATION TO ATC RADARS

TECHNICAL DOCUMENTARY REPORT NO. ESD-TDR-64-518

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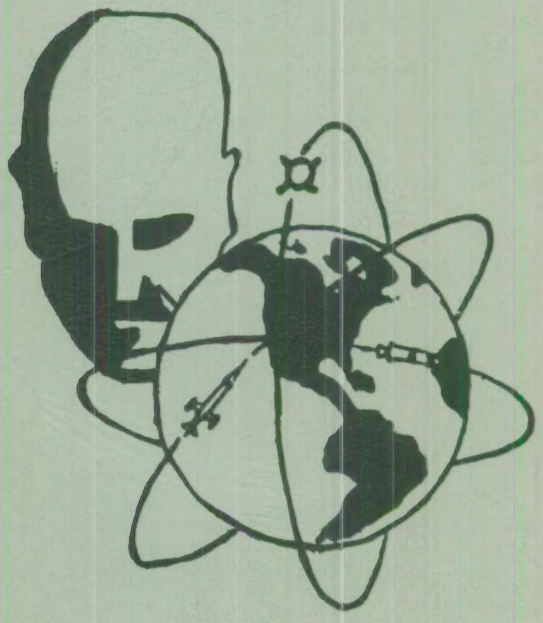

System 482L

(Prepared under Contract No. AF 19 (604)-8854 by the AVCO Corporation, Electronics Division, Cincinnati, Ohio.)

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THE DESIGN, DEVELOPMENT AND EVALUATION OF IMPROVED STC EQUIPMENT FOR APPLICATION TO ATC RADARS

A B S T R A C T

The need for improved Sensitivity Time Control circuits in Air Traffic Control radar equipment becomes more imperative as Emergency Mission System search and precision radars become more sensitive and all-weather tracking and controlling to within a mile of the radar site becomes standard procedure.

This report traces the development of a sophisticated logarithmic STC circuit from previously derived concepts through incorporation in, and evaluation of, the latest EMS search radar.

The development of Digital Video Data processing equipment led to design and experimental work on a digital STC concept. The preliminary investigation of this concept indicates that a significant advance in this direction is possible in clutter attenuating devices.

Reference is also made to the current EMS system including test results plus recommendations for improvements in anti-clutter devices for present and future search and precision radars.

Technical documentary report ESD-TDR-64-518 has been reviewed and is approved.

H. M. KNIGHT
Technical Monitor, AF19(604-8854
Hq ESD (ESRRG)

F O R W A R D

The entire effort described in this report was performed by the contractor at the customer's facility located at Fort Dawes, Winthrop, Massachusetts. This work was done under the general direction of Mr. Herbert M. Knight, Assistant Chief, Technical Support Division of 482L/431L SPO. The authors are indebted to him for the stimulating discussions held during the progress of this program and for his helpful suggestions and criticisms.

KEY WORD LIST

1. AIRPORT RADAR SYSTEMS
2. DESIGN
3. TESTS
4. INTERFERENCE
5. DATA PROCESSING SYSTEMS

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED) . . . .

LIST OF ILLUSTRATIONS

List of Illustrations (Cont'd).....

SECTION 1

INTRODUCTION

The following material is presented as background to facilitate a better understanding of the problem areas under consideration.

As the speed of present day aircraft increases, it becomes necessary to provide Air Traffic Control centers with better radar coverage. This is accomplished by increasing the sensitivity of the radar set, thereby extending its range and altitude capabilities. While this provides the added coverage desired, the radar also becomes more sensitive to ground clutter, moving ground vehicles, and small targets such as birds in flight. The problem varies with terrain surrounding the site but is greatest in the vicinity of large cities. For this reason, the optimum setting for clutter versus target sensitivity usually varies with azimuth as well as range at a given location.

The close-range clutter problem has been given considerable study in the past, and the problem has been approached in several ways. Four of these approaches are discussed briefly below.

1. Tilt the antenna back to obtain the optimum compromise between low angle detection and ground clutter. While it might be possible to achieve a satisfactory angle between antenna beam and ground for one direction, it would most certainly not be the optimum setting in all directions, since ground clutter varies with azimuth. This approach would necessarily cause a greater loss of targets under the main beam and thereby make it even more difficult to detect low-flying aircraft.

2. The most successful method thus far employed to eliminate ground clutter is the use of moving target indication equipment. However, there is a limit to the amount of stationary target rejection possible with MTI. With very sensitive radars, the magnitude of stationary target returns in a metropolitan area is often so high that significant residue remains even after cancellation. Furthermore, birds and moving surface traffic within the radar beam can have sufficient velocity to prevent them from being cancelled.

3. Various types of video processing equipment have been used to improve target detection. Systems which process video from the radar receiver are only as good as the information they receive. Systems that use the principle of detecting the difference in amplitude between clutter residue and targets, or that determine the existence of a target by counting the number of repeated signals in a given range increment over several consecutive sweeps, have the tendency to eliminate real targets due to saturation in the receiver.

4. The use of Sensitivity Time Control circuitry in conjunction with MTI equipment has been given some consideration. The earlier that the incoming radar information is processed to improve the signal-to-noise ratio, the less one must contend with limits imposed on the video by the receiving system. Since, in general, the close-in target returns of interest reach the receiver at a much higher magnitude than would be necessary for clear display in the absence of ground clutter, reduced receiver gain during that period of time could greatly reduce MTI residue while still permitting low antenna angle

and adequate target reflection. Therefore, it was felt that some form of STC could be of considerable aid in improving the signal-to-noise ratio in the MTI receiver; thus making it easier to distinguish targets from noise and clutter.

STC is a device to dynamically adjust the receiver gain during each radar range sweep so as to attenuate signals at close ranges. In most instances, there is a proper attenuating value which will greatly reduce or eliminate the MTI clutter residue, but will not entirely wipe out an aircraft signal. This attenuating value is a function of the range and azimuth location of the aircraft and the amount of clutter residue present. Two approaches utilizing STC principles are examined in subsequent sections of this report. Section 2 is devoted to a logarithmic STC unit and Section 3 covers a Digital Video Data Processor.

SECTION 2

LOGARITHMIC STC DEVELOPMENT & EVALUATION

A. GENERAL

When STC was first incorporated in radars, a single RC recovery characteristic, initiated by the system trigger (Figure 1A, Page 5), was used as an approximation of the theoretical control function (Figure 1B). An early modification was to clip the initial portion of the function, resulting in a flat section prior to the start of the recovery slope (Figure 1C). The particular RC time constant to be used, its magnitude, and the duration of the initial flat portion, were determined experimentally resulting in a crude approximation of the optimum curve. Another disadvantage of early STC circuits is the interaction of the various controls required to establish the shape of the curve. This interaction made rapid adjustment impossible. Due to these factors, targets were lost through excessive attenuation in some areas, while in other areas, excessive uncancelled clutter remained.

B. DEVELOPMENT

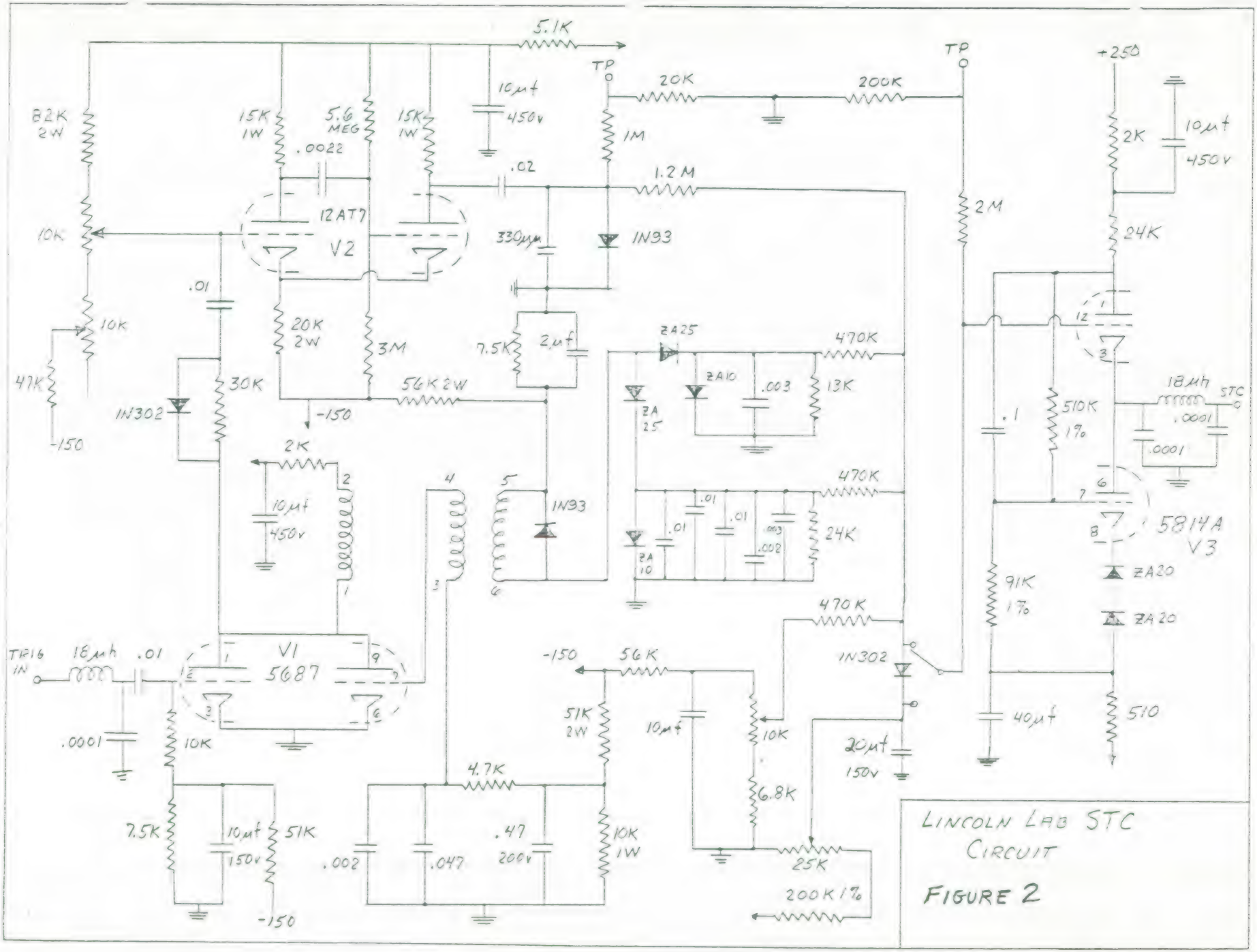
The ideal control function is one which gives a receiver voltage gain that varies as the square of the range (see Reference 5 in Bibliography). This concept, derived by Lincoln Laboratory, was designed into a STC unit which presented improvements over earlier circuits (Figure 2, Page 6). This unit more closely matched the characteristics of the I-F strip which it controlled so as to provide

[A] Radar Trigger

[B] Single RC Time Constant

[C] Single RC Time Constant Plus Initial Clipping

FIGURE 1: DEVELOPMENT OF EARLY STC FUNCTION


5.1K
TP
10μf 450v
20K
200K
TP
+250
B2K 2W
15K 1W
5.6 MEG
15K 1W
.0022
.02
1M
1.2 M
2M
2K
10μf 450v
24K
12AT7 V2
330μμ
IN93
10K
.01
10K
20K 2W
3M
7.5K
2μf
ZA25
470K
ZA10
.003
13K
47K
-150
IN302
30K
56K 2W
-150
ZA 25
18μh
STC
.0001
.0001
.1
510K 1%
2K
10μf 450v
470K
.01
.01
.01
.003
.002
24K
ZA 10
5814A V3
91K 1%
ZA20
ZA20
TRIG IN
18μh
.01
V1 5687
470K
-150
56K
IN302
51K 2W
10μf
10K
6.8K
20μf 150v
40μf
510
.0001
10K
4.7K
7.5K
10μf 150v
51K
.002
.047
.47 200v
10K 1W
25K
200K 1%
-150
LINCOLN LAB STC CIRCUIT
FIGURE 2

a 12db per octave gain control over 4 octaves of range. This characteristic provided an attenuation which is directly proportional to the signal voltage received at the radar from targets within the main antenna beam at all ranges over the 4 octaves. This desired function slope was obtained by the addition of two exponentially decaying pulses of different time constants. The Gain Control settings were non-interacting and did not effect the shape of the theoretically optimum curve. The circuit included an adjustable range-gate to restore the receiver sensitivity to a predetermined maximum value as each sweep reached a selected range. This unit was designed for use with a radar having negatively grid biased tubes in the I-F strip and for general search radar applications it is excellent.

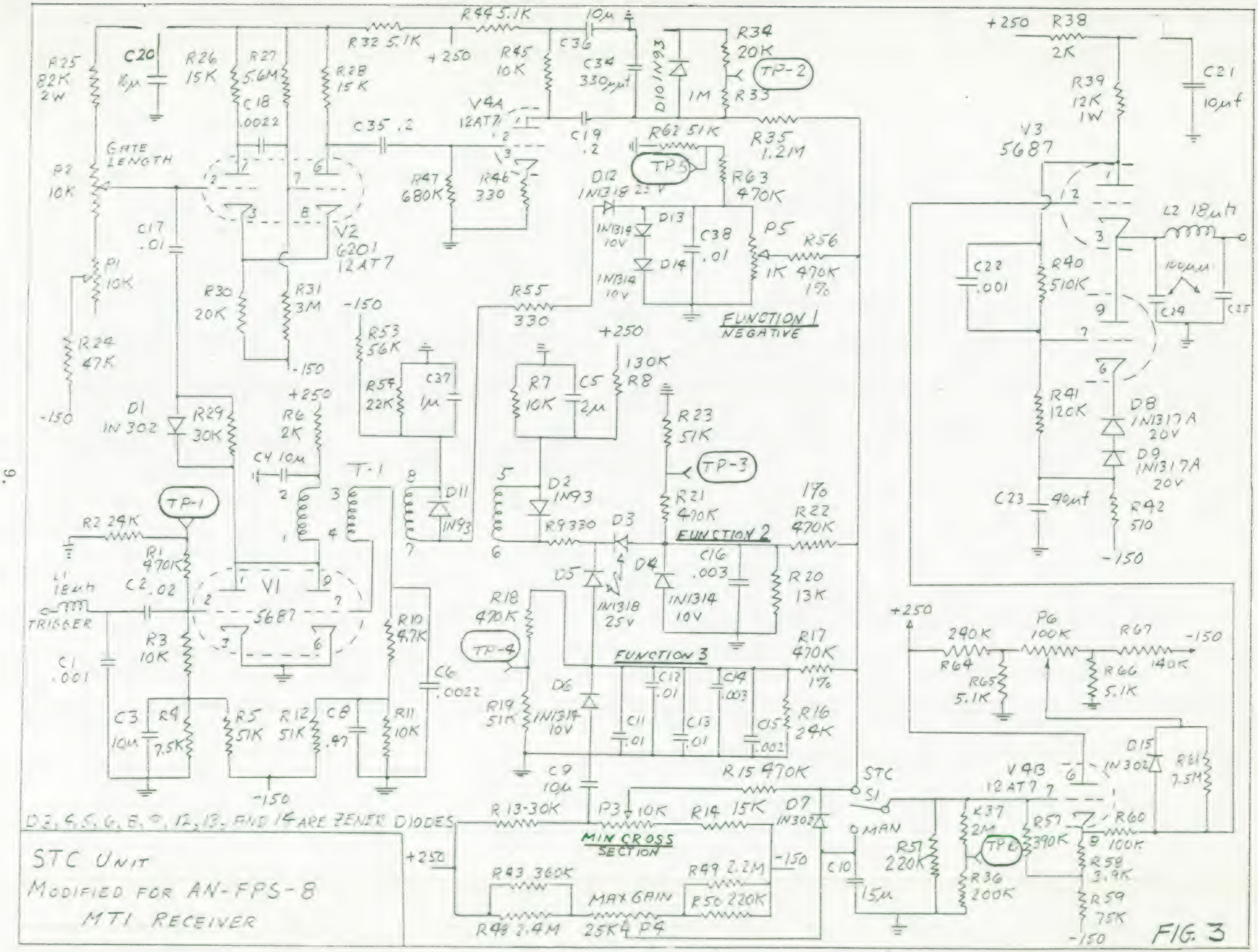
Our main interest is to improve the video presentation for air traffic control operation. The above mentioned circuit was designed for grid control of the first two stages of an I-F strip, and the AN/FPS-8 radar, used here for experimentation , has the control voltage applied to the cathodes in its I-F amplifier. Therefore, either the I-F strip had to be modified for grid control, or the waveform out of the STC unit would have to be inverted to be applied to the cathodes.

Since it was easier to redesign the STC unit then to require future radar modifications in the field, the former choice was made. Briefly, this was accomplished by an inversion of all the function generators, and by a change of the cathode follower output tube from a 5814 to a 5687 to handle the additional current in the cathode circuit of the I-F amplifier. The slope of the waveform was changed to match the

characteristic of the AN/FPS-8 I-F strip so as to provide the 12 db per octave gain control characteristic desired. To achieve the desired gain per range slope, the peak value of the composite exponential function in the 1 to 4 mile region produced so much receiver attenuation as to eliminate all targets in that interval. It was felt that this 1 to 4 mile region should be improved, since frequently aircraft within this range will be flying under the main beam of the radar. Aircraft may also be flying under the main beam at longer ranges when they are in the vicinity of reporting points and holding fixes at the minimum altitude, or are proceeding outbound at minimum altitude until they cross an airway. To solve this problem, the positive going STC developed for use with the AN/FPS-8 radar located at Fort Dawes has been improved in the following manner. In addition to the composite exponential function, the improved circuit (see Figure 3, Page 9) has two means of achieving optimum setting of gain in the 1 to 4 mile range. The first of these is a negative going exponential function to limit the initial peak excursion of the STC function. The second is an adjustable clipping circuit permitting a near flat limiting of STC gain reducing voltage to a desired maximum level during the first several miles of range. This unit was then tested in conjunction with the AN/FPS-8 radar and the results indicated a definite improvement in the 1 to 4 mile range interval.

C. CIRCUIT DESCRIPTION

Again, referring to Figure 3 and the block diagram shown in Figure 4, the main bang radar trigger is fed into blocking oscillator V-1. The


STC UNIT
MODIFIED FOR AN-FPS-8
MTI RECEIVER
D2, 4, 5, 6, 8, 9, 12, 13, AND 14 ARE ZENER DIODES
FUNCTION 1
NEGATIVE
FUNCTION 2
FUNCTION 3
MIN CROSS SECTION
MAX GAIN
TRIGGER
GATE LENGTH
STC
MAN
5687
12AT7
6201
IN302
IN93
IN1314 10V
IN1318 25V
IN1317A 20V
TP-1
TP-2
TP-3
TP-4
TP-5
TP-6
+250
-150
FIG. 3

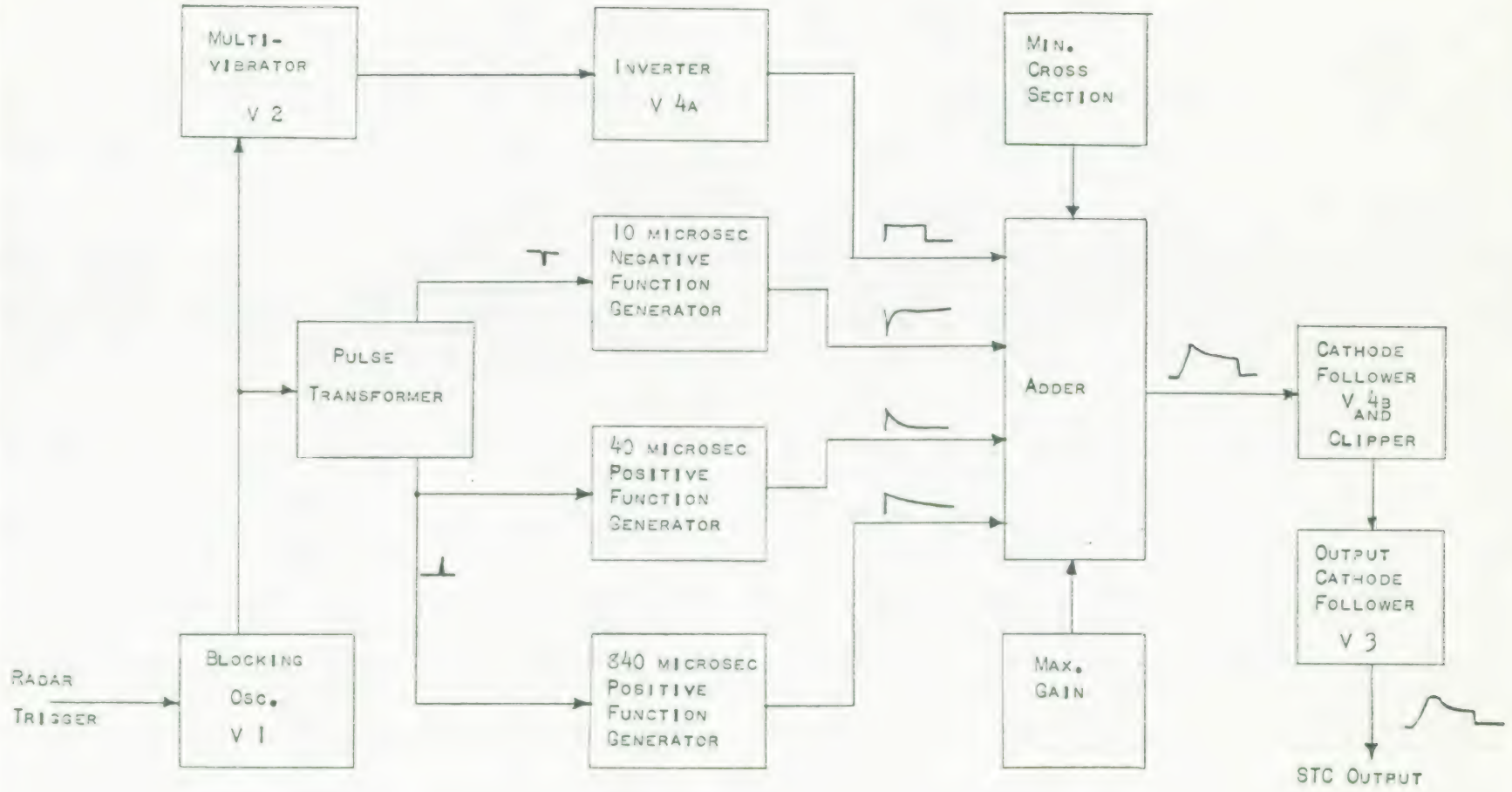


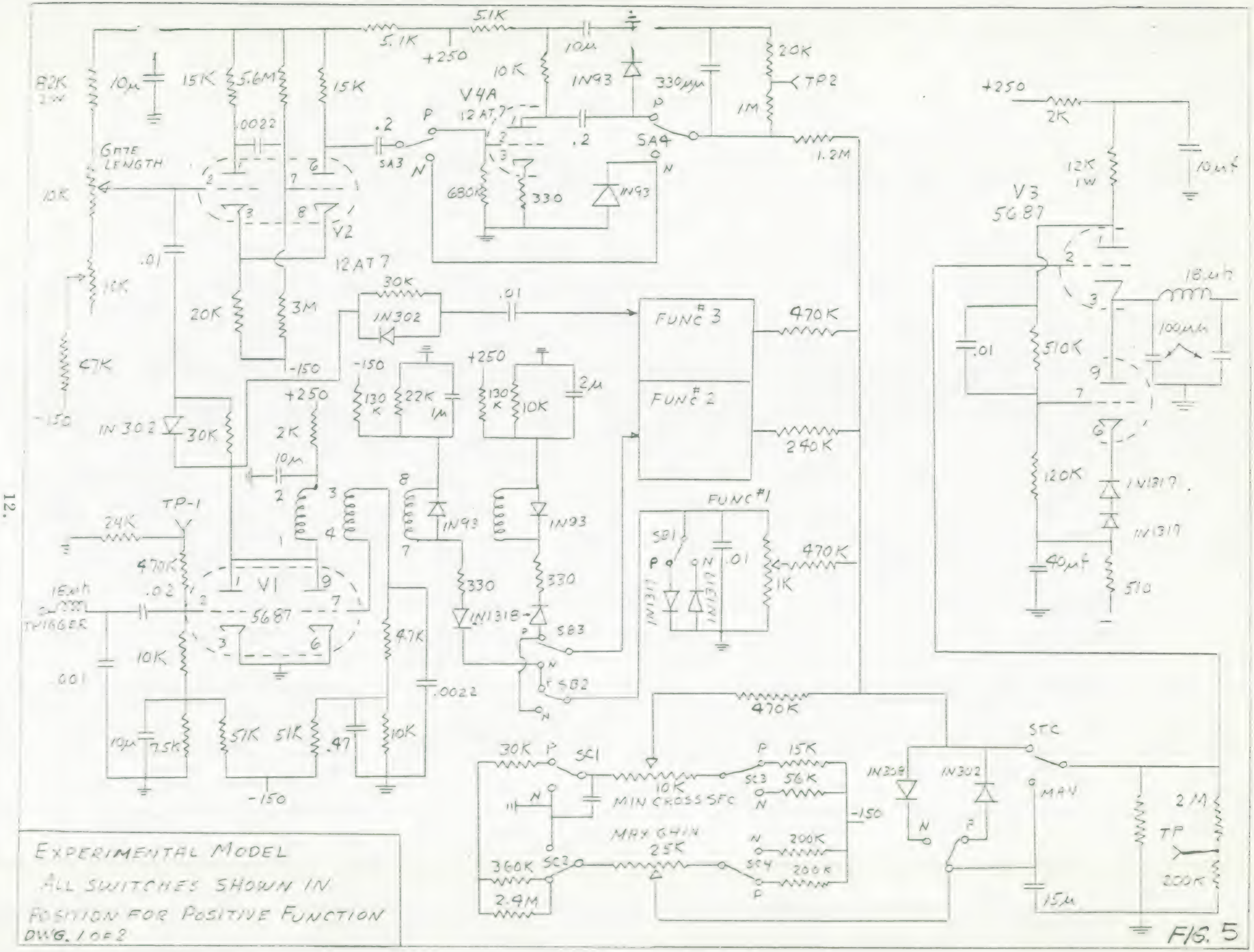
FIGURE 4: STC UNIT BLOCK DIAGRAM

positive and negative pulses taken from the windings of pulse transformer T-1 charge up the capacitors in the various function generators to the value determined by the zener diodes used. The R-C time constant of each function generator determines the slope of its waveform. The trigger out of the blocking oscillator also fires a one-shot multivibrator V-2, which supplies the range gate to restore the receiver to maximum gain at some preset range. These functions are summed with the DC level gain controls to supply the composite STC waveform. The two positive functions provide the desired gain control characteristic while the negative function furnishes some compensation for the T-R recovery time period. The minimum cross section shifts the STC waveform level while the maximum gain control sets the level beyond the end of the range gate. A clipping circuit on the output of cathode follower V-4B produces the flat portion of the waveform during the initial few miles of range. The cathode follower V-3 permits the output to be shifted above or below ground level, without distorting the shape of the curve, and can supply the current demands for cathode biasing the tubes in the I-F strip.

D. OTHER ANALOG APPROACHES

While the above type of analog STC generator appears to be the most satisfactory at the moment, other methods of generating STC waveforms have been looked into. Some thought has been given to having the shape of the STC curve vary not only as a function of range, but also as a function of azimuth. The following two circuits have been breadboarded and tested.

The first circuit, Figures 5 & 6, Pages 12 & 13, has the facility of

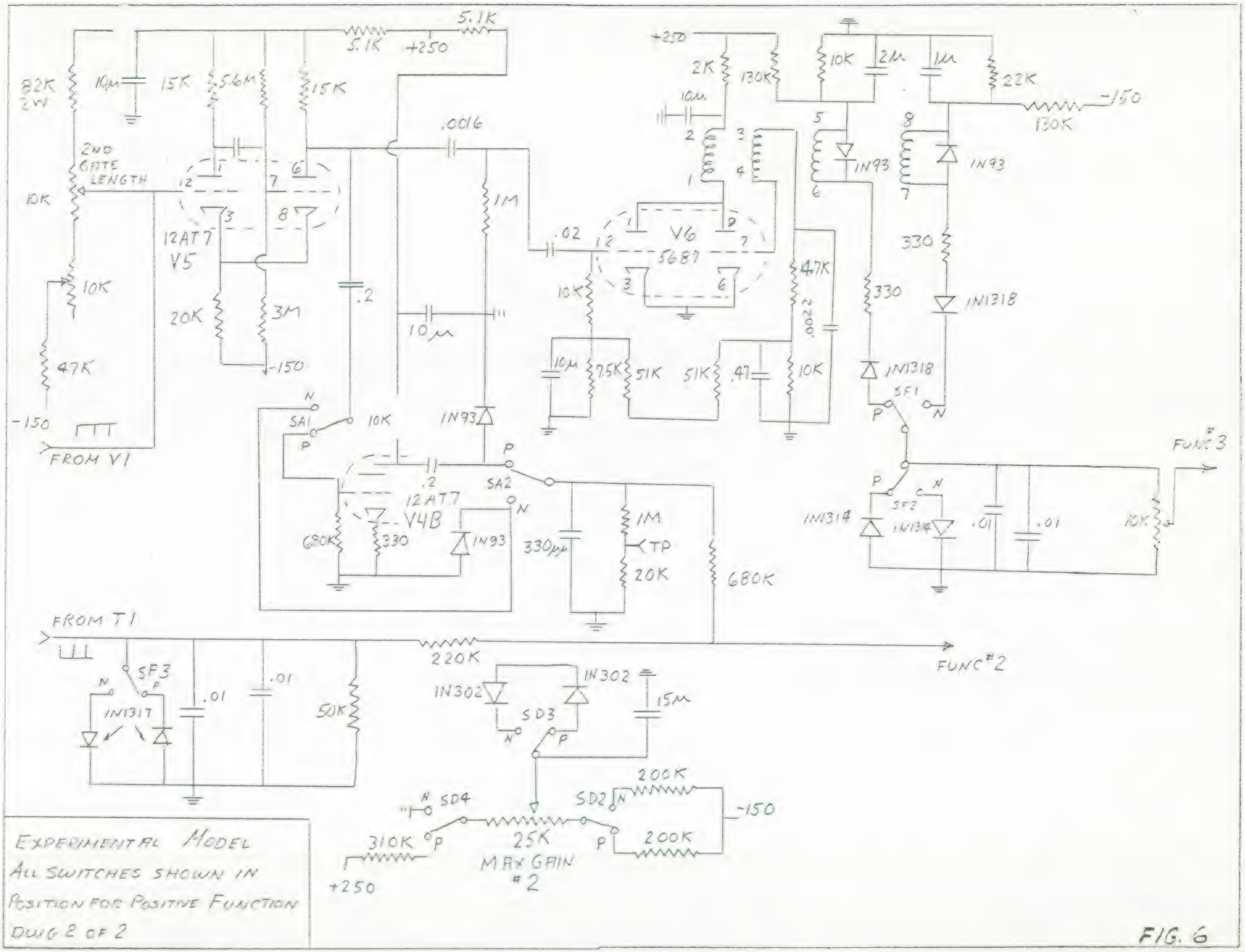


EXPERIMENTAL MODEL

ALL SWITCHES SHOWN IN POSITION FOR POSITIVE FUNCTION

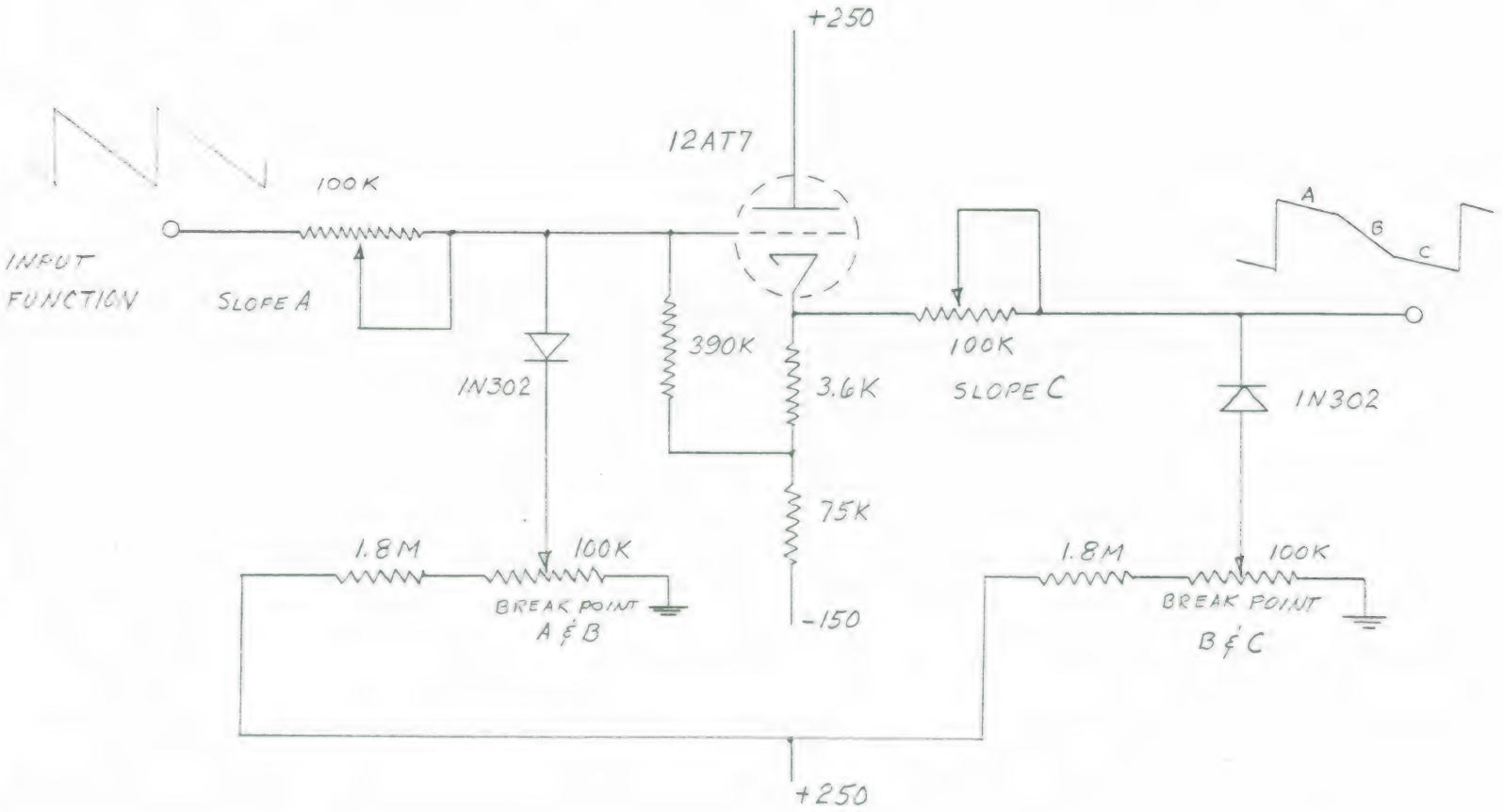
DWG. 1 OF 2

FIG. 5



EXPERIMENTAL MODEL
ALL SWITCHES SHOWN IN POSITION FOR POSITIVE FUNCTION
DWG 2 OF 2

FIG. 6



WAVE SHAPING CIRCUIT
STC

FIG. 7

initiating different functions for the composite waveform at different ranges controlled by an adjustable range gate. Since this unit was built for experimental purposes, it was designed to furnish either a positive or negative going signal so that, if desired, it could be used in conjunction with various radars regardless of whether their I-F amplifiers are cathode or grid biased. The circuit performed as designed; however, due to the number of controls required to adjust the various sections of the curve, it was considered too complicated for practical use. It is apparent that if the range gate, which determines the end of one function and the start of another, was varied as a function of azimuth, there would have to be several adjustments which would also be dependent on azimuth to give a smooth continuity between the two portions of the curve.

The second circuit, Figure 7, Page 14, is a wave shaping device into which a predetermined exponential curve or sawtooth may be introduced. With this circuit, two break points are established dividing the input slope into three segments. These break points can be moved in range and the slopes of the two end segments can be independently adjusted. Again, varying these controls as a function of azimuth to fit various terrains, would not be practical.

E. RESULTS AND EVALUATION

To use this STC function in conjunction with the AN/FPS-8, the following modifications had to be made to the MTI IF amplifier:

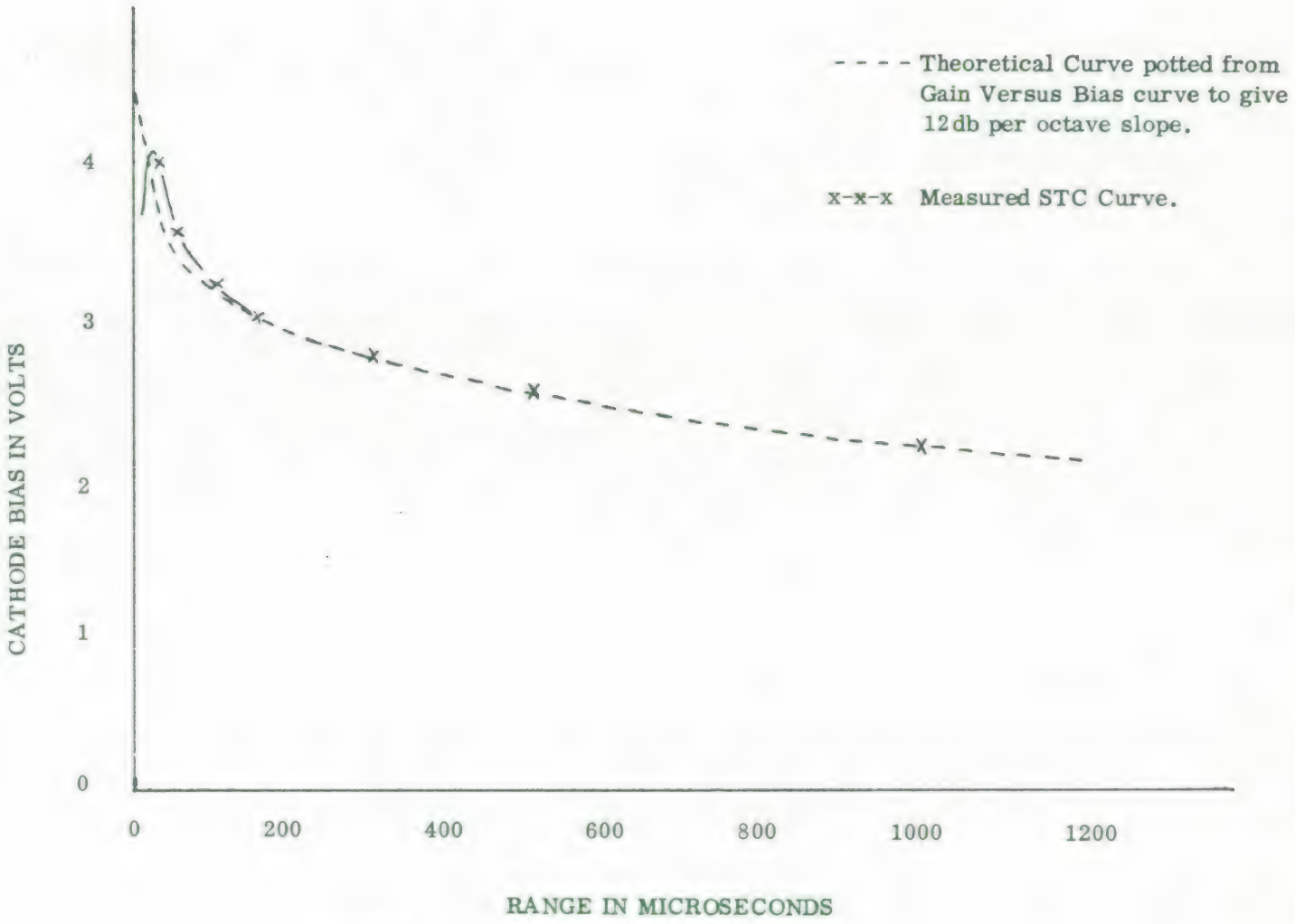


FIGURE 8: BIAS VERSUS RANGE

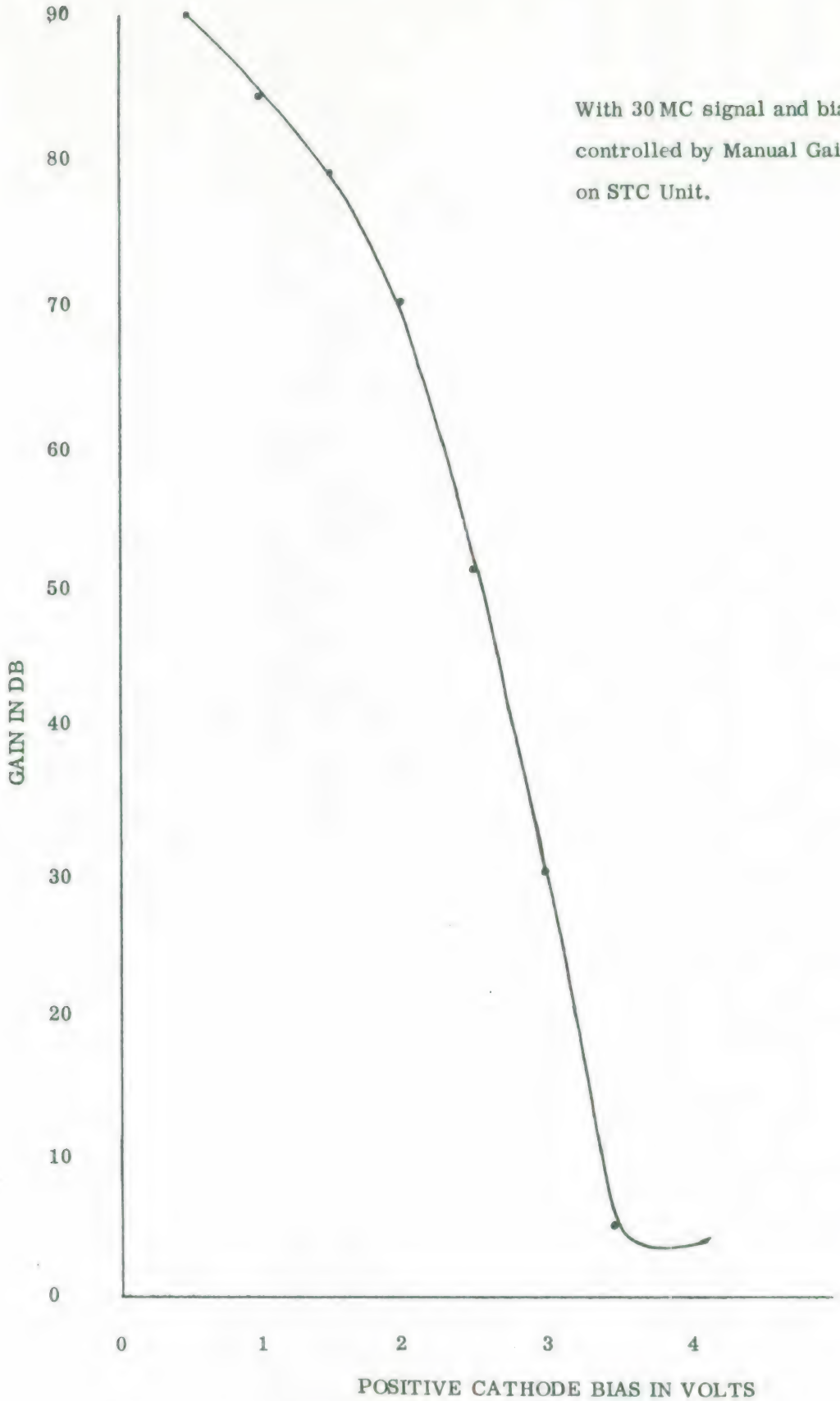


FIGURE 9: GAIN VERSUS BIAS OF AN/FPS-8 IF

RANGE IN MICROSECONDS	40	80	160	320	640	1280
GAIN IN DB	10	23	37	49	60	66
CHANGE IN GAIN DB/OCT		13	14	12	11	6
WAVEFORM OF 40 MICROSEC + 840 MICROSEC, SET FOR 2.55V AT 500 MICROSEC						

FIGURE 10: Change in Gain, DB Per Octave

1. The present source of positive bias was disconnected and a BNC jack installed. This permitted the connection of the STC output through a 330 ohm resistor to the bias line as a new source of gain control.
2. A 1.0 microfarad capacitor was connected from ground to the point of B+ source nearest the two tubes whose bias the STC controlled. This decreased the modulating effect of the STC waveform on the 30 mc carrier in the I-F strip.

The best operational results on the AN/FPS-8 at Fort Dawes were obtained with a minimum cross section setting which positioned the STC curve so that it measures 2.55 volts at 500 microseconds after the initiating trigger. As can be seen in Figure 8, Page 16, this is in close agreement with the theoretical STC curve derived to match the gain characteristic of the I-F strip which is shown in Figure 9, Page 17. The minimum cross section can be adjusted up or down, but there is a loss of linear dynamic range, due to the non-linearity of the I-F gain characteristic at the two extremes. That is, as the STC curve is shifted down, the shorter ranges are controlled on the steeper slope of the I-F gain curve, thereby having a greater change in gain for a given change in STC voltage. Since there are only about four 12db segments of the gain curve which are reasonably linear, this does not leave much room for minimum cross section adjustment. At what appeared to be the optimum setting mentioned above, 4 octaves of approximately 12 db/octave gain control were obtained as noted in Figure 10 on Page 18.

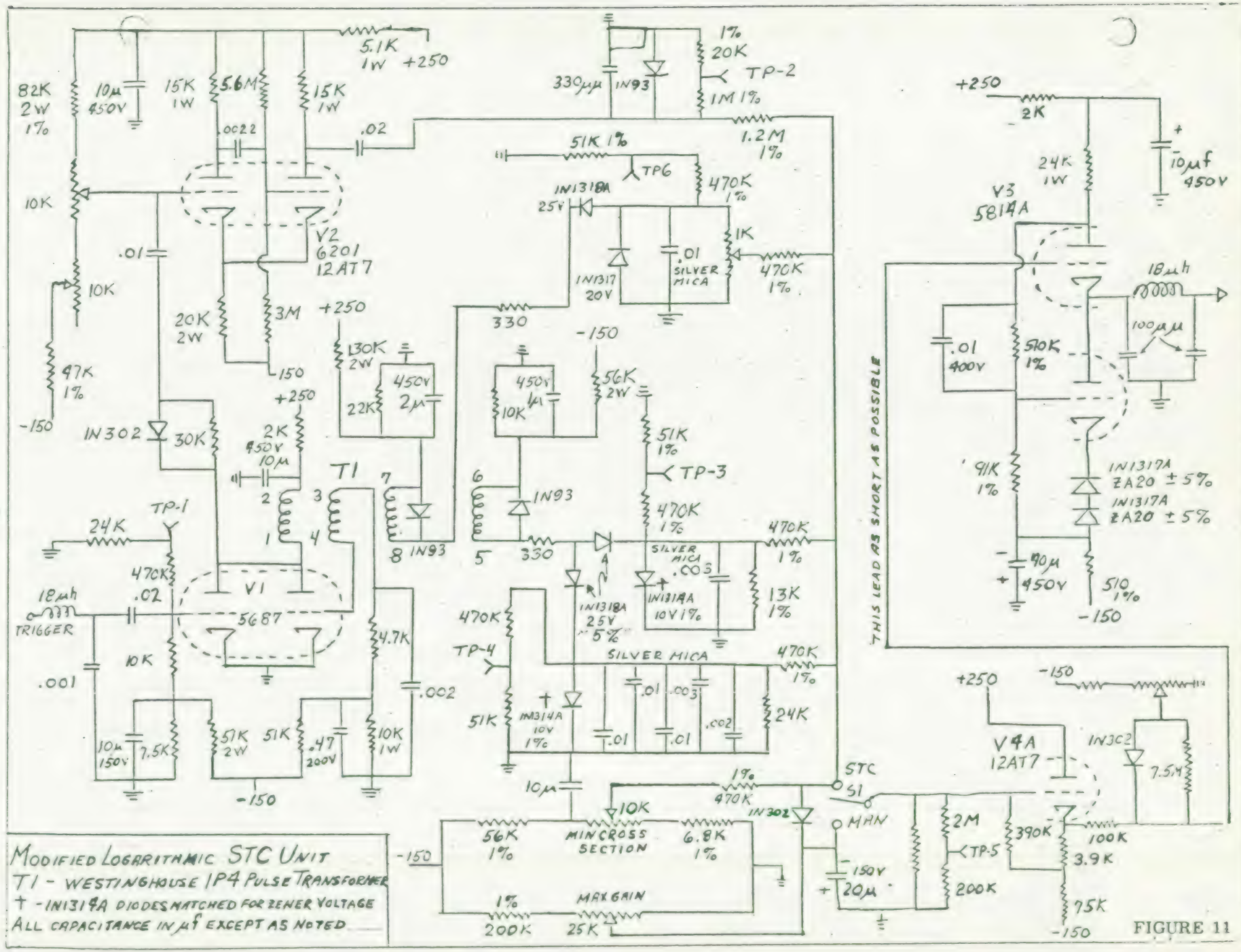
F. APPLICATIONS

Figure 11, Page 21, is the schematic of a unit to generate a negative STC function. This unit incorporates all the previously mentioned improvements. While this unit was never breadboarded, it shows the necessary changes to supply a grid controlling logarithmic STC waveform. This developmental work resulted in the incorporation of the requirements for this type STC unit in the Military Specifications for the AN/TPS-35 search radar. The AN/TPS-35 is part of the AN/TSQ-47 Air Traffic Control System. The unit was installed in almost the same form as described and shown here. Enclosed on Page 23, Figure 13, is the circuit as it appears in the AN/TPS-35 manual.

Data on the AN/TPS-35 indicates that the results obtained were very similar to that shown in Figure 10. The data presented on Page 22, Figure 12, is from the system performance tests on the three AN/TPS-35 radars.

G. CONCLUSIONS

The logarithmic STC circuit shown in Figure 3, is as far as one can go with a practical analog function. Much thought was given to ways of having a logarithmic waveform vary as a function of azimuth. The simplest way to do this would be to divide the area circumscribed by the limits of radar coverage into a number of sectors and have several STC waveforms which could be switched in and out with cam switches operated by a shaft synchronized with the antenna rotation. Another way would be to use non-linear pots which would vary the time constants in the function generators as a function of azimuth. Among


MODIFIED LOGARITHMIC STC UNIT
T1 - WESTINGHOUSE IP4 PULSE TRANSFORMER
† - IN1314A DIODES MATCHED FOR ZENER VOLTAGE
ALL CAPACITANCE IN μf EXCEPT AS NOTED
THIS LEAD AS SHORT AS POSSIBLE
MIN CROSS SECTION
MAX GAIN
TRIGGER
TP-1
TP-2
TP-3
TP-4
TP-5
TP6
V1
5687
V2
6201
12AT7
V3
5814A
V4A
12AT7
T1
IN302
IN93
IN1318A
IN1317
IN1317A
IN314A
IN3C2
SILVER MICA
STC
S1
MAN
+250
-150
FIGURE 11

	RANGE IN MICROSECONDS	50	100	200	400	800
System 1	GAIN IN DB	21.8	36.8	49.9	60.0	70.0
	CHANGE IN GAIN DB/OCTAVE (REMOTE)		15	13.1	10.1	10
2	GAIN IN DB	2.0	14.2	26.2	38.2	50
	CHANGE IN GAIN DB/OCTAVE (LOCAL)		12.2	12	12	11.8
3	GAIN IN DB	12	26	37	47	60
	CHANGE IN GAIN DB/OCTAVE (REMOTE)		14	11	10	13

FIGURE 12: AN/TPS-35 STC DATA

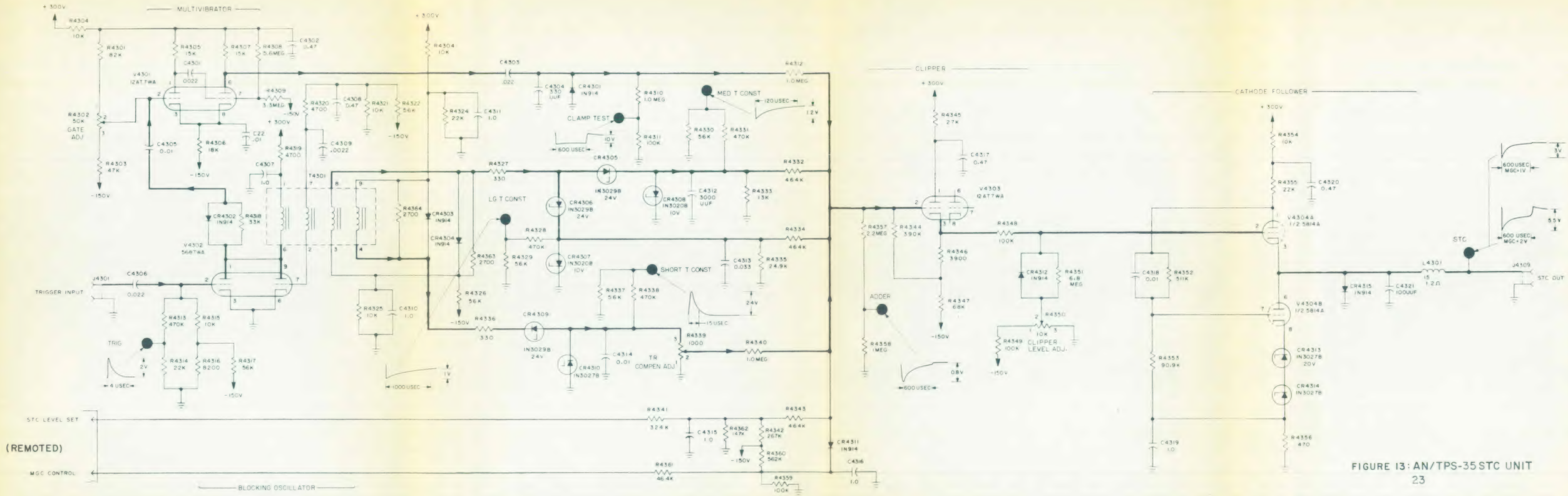


FIGURE 13: AN/TPS-35 STC UNIT

the disadvantages of these methods are the expense, the physical size of multiple equipment, and the large number of adjustments necessary. This type of system would have no way of adapting itself to compensate for varying conditions such as atmospheric changes. Also, since these functions are only an average curve for any one range sweep, they would not compensate for the varying density of ground clutter. The final logarithmic STC circuit which evolved from this work is therefore the most practical.

SECTION 3

DIGITAL STC DEVELOPMENT AND EVALUATION

A. GENERAL

The analog circuits presented in SECTION 2 do not readily permit varying the STC waveform as a function of azimuth. The ultimate in STC circuitry would generate a sweep-by-sweep bias control voltage as a function of the returning signals. One way to approach this was to have the STC voltage be a function of the video from several preceding sweeps. To accomplish this, a Digital Video Processor available at Fort Dawes was modified to provide outputs which, through additional circuitry, would produce this type of STC waveform. This now permitted the STC voltage to vary as a function of azimuth. That is, the voltage level for each half mile interval was now dependent on the density of the signals received in that half mile increment during the previous 16 radar range sweeps.

This Digital Video Processor accepts radar video and converts all signals above a predetermined level to standard 6 volt pulses. Sixty-four miles of this data is resolved into 128 one-half mile increments. Using a memory unit, the 16 previous bits of information for each of the 128 one-half mile increments are stored. When the memory is "read" the 16 bits of information in each one-half mile increment are "read" and summed. The above method is used to continuously scan and sum information in azimuth. By similar circuitry, 7 one-half mile increments are scanned in range.

The result is a continuously scanning sampling cell, 16 triggers wide in azimuth, and three and one-half miles long in range. A statistical analysis, based on the density of the information, establishes whether the signal returns are caused by aircraft, ground clutter, noise, interference, weather, etc. Those signals identified as targets are the output of the processor. This processor was developed on Air Force Contract No. AF 19(604)-8479.

A more complete description of the principles of operation of the processor and a logic diagram are contained in a report entitled "Solid State Radar Data Processor - Final Report", by F. A. Epsom of Rescon Electronics Corporation, Waltham, Massachusetts, October 25, 1961. Appendix A contains an expanded and more detailed explanation of the logic and circuitry used in the processor, plus complete schematics. This Appendix was written by the author so that the reader could have better understanding of the processor and its subsequent use in the digital STC circuitry.

B. DEVELOPMENT

The approach taken was to sum the information outputs of the 12 previous range sweeps, which were stored in the core memory to supply a basic STC waveform. Thus, the amount of gain reduction is proportional to the amount of information stored in any one-half mile segment. It was necessary to generate a positive going STC waveform, since the unit was to be tested on a radar set whose receiver utilized cathode biasing in the IF stages. The inverted output of the processor, corrected in

time to be in coincidence with the radar video, was added to this basic waveform, thereby increasing the gain within those range segments that the processor thought contained a target. Since the processor is accurate to one-quarter mile and the target output is only 1.8 microseconds wide, provisions had to be made to widen the targets to one-quarter mile (3 microseconds) to insure that the aircraft signal receives the benefit of the system. In other words, the STC gain controlling characteristic was directly proportional to the density of signal returns and inversely proportional to the signals which the processor has established as targets.

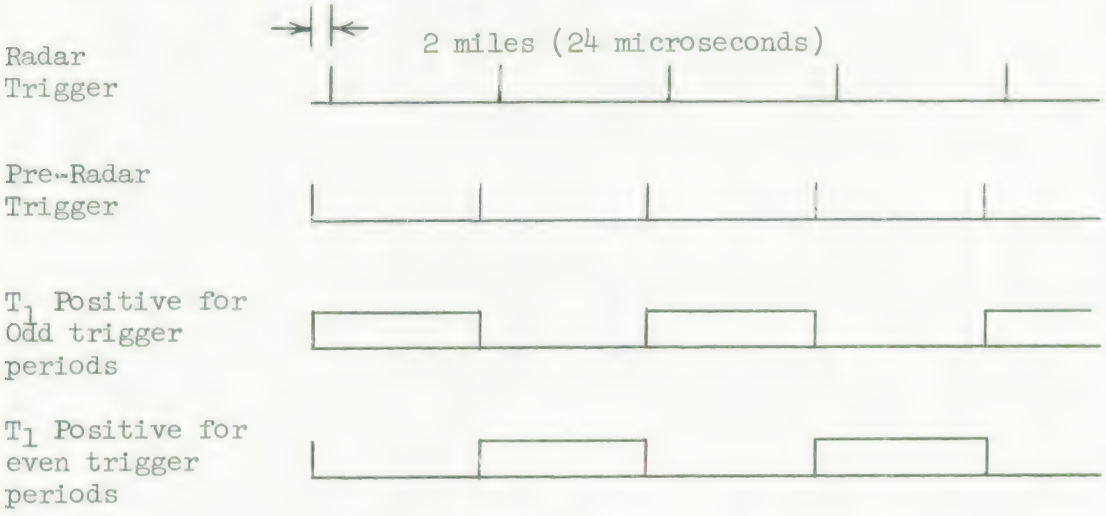
In adapting this processor for use as a source of information to establish a STC waveform, one had to first take into consideration the time delays inherent in the unit. Before the quantized video is fed into the Memory Unit, a half-mile of delay has accummulated. In the automatic mapping section, another one and one-half mile delay occurs. This means that if the memory outputs are summed, this summation will be one-half mile late. Since the processor output will then be still another one and one-half miles later, something had to be done to have these two sources of information coincide in time with the radar information of a later range sweep.

To achieve this, the quantized video has been fed, on alternate sweeps, into two series shift registers (of 128 flip-flops each) clocked with quarter mile pulses. Each register is capable of storing 32 miles of information in quarter mile segments, thereby preserving

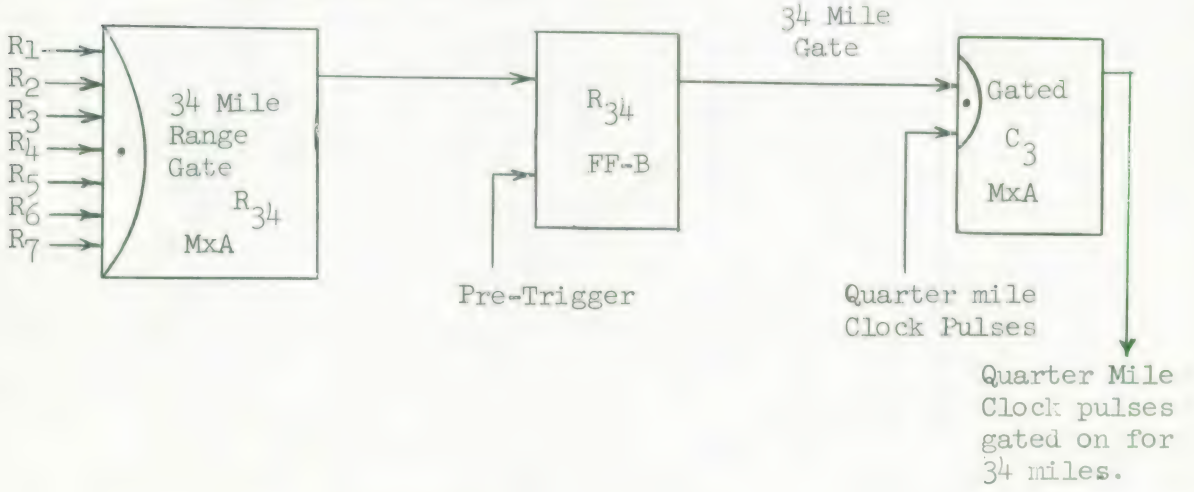
the half mile resolution and quarter mile accuracy of the system. These registers are then emptied alternately by a series of pulses initiated by a pretrigger set to compensate for the processor delay. The same effect can be obtained without a pretrigger by permitting 34 miles of data to be fed into the registers capable of storing only 32 miles of data. As the register fills during one sweep, the first two miles of information is dumped out the other end. The clock pulses then stop and the data is stored for the remainder of the range sweep. When the register is emptied during the next sweep, the information will be clocked out two miles early. After the delays in the processor, the output video will be in coincidence with the radar video, but with an absence of the first two miles of data. If a pretrigger is used, the shifting will start 24 microseconds early and the first two miles of data will be preserved. Delaying the twelve memory outputs by one and one-half miles will then put their summation in coincidence with the radar.

C. CIRCUIT DESCRIPTION

1. Within the processor is a series of flip-flops which count down triggers and provide gates which can be used to alternately turn on and off the two series shift registers for storing alternate sweeps of quantized data in quarter mile increments.



2. The quarter mile clock pulses will be initiated by the pre-trigger to shift the storage registers. They then must be stopped at 34 miles (2 miles before data plus 32 miles of data) or the register will be emptied too soon.



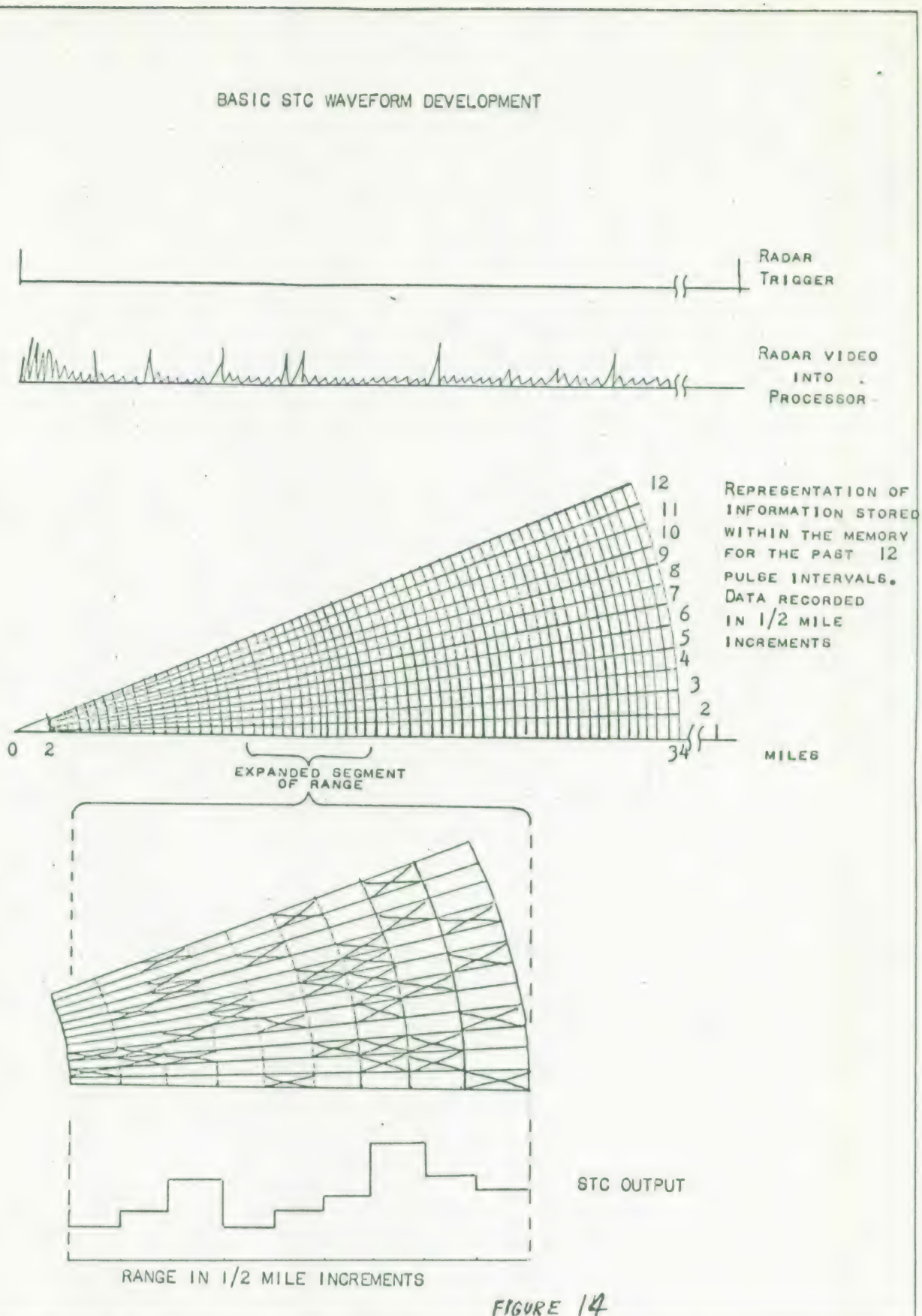
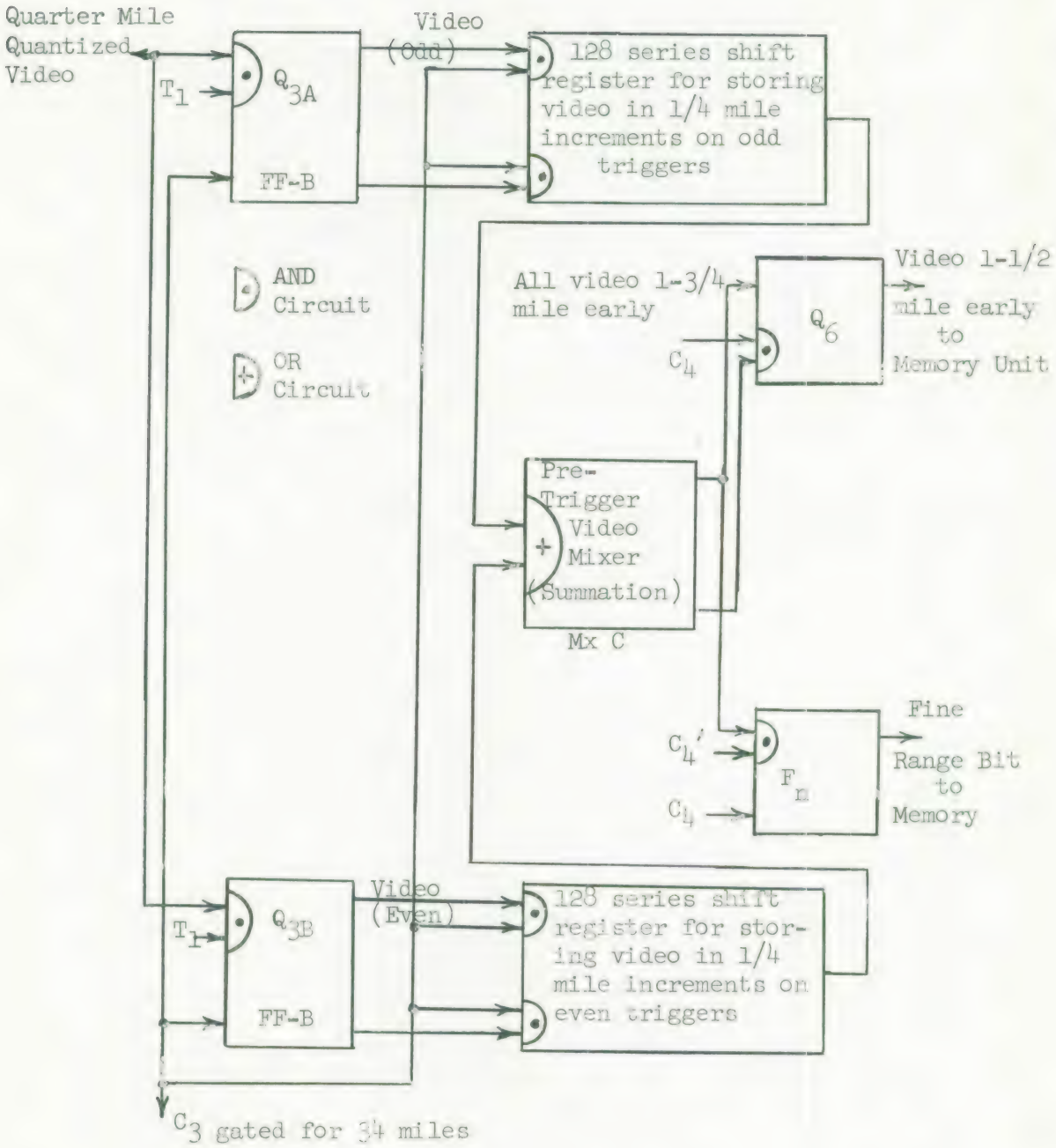

BASIC STC WAVEFORM DEVELOPMENT
RADAR TRIGGER
RADAR VIDEO INTO PROCESSOR
12
11
10
9
8
7
6
5
4
3
2
1
REPRESENTATION OF INFORMATION STORED WITHIN THE MEMORY FOR THE PAST 12 PULSE INTERVALS. DATA RECORDED IN 1/2 MILE INCREMENTS
0 2
34
MILES
EXPANDED SEGMENT OF RANGE
STC OUTPUT
RANGE IN 1/2 MILE INCREMENTS

FIGURE 14


Quarter Mile Quantized Video
T_1
Q_{3A}
FF-B
Video (Odd)
128 series shift register for storing video in 1/4 mile increments on odd triggers
AND Circuit
OR Circuit
All video 1-3/4 mile early
C_4
Q_6
Video 1-1/2 mile early to Memory Unit
Pre-Trigger Video Mixer (Summation)
Mx C
C_4'
C_4
F_n
Fine Range Bit to Memory
T_1
Q_{3B}
FF-B
Video (Even)
128 series shift register for storing video in 1/4 mile increments on even triggers
C_3 gated for 3/4 miles

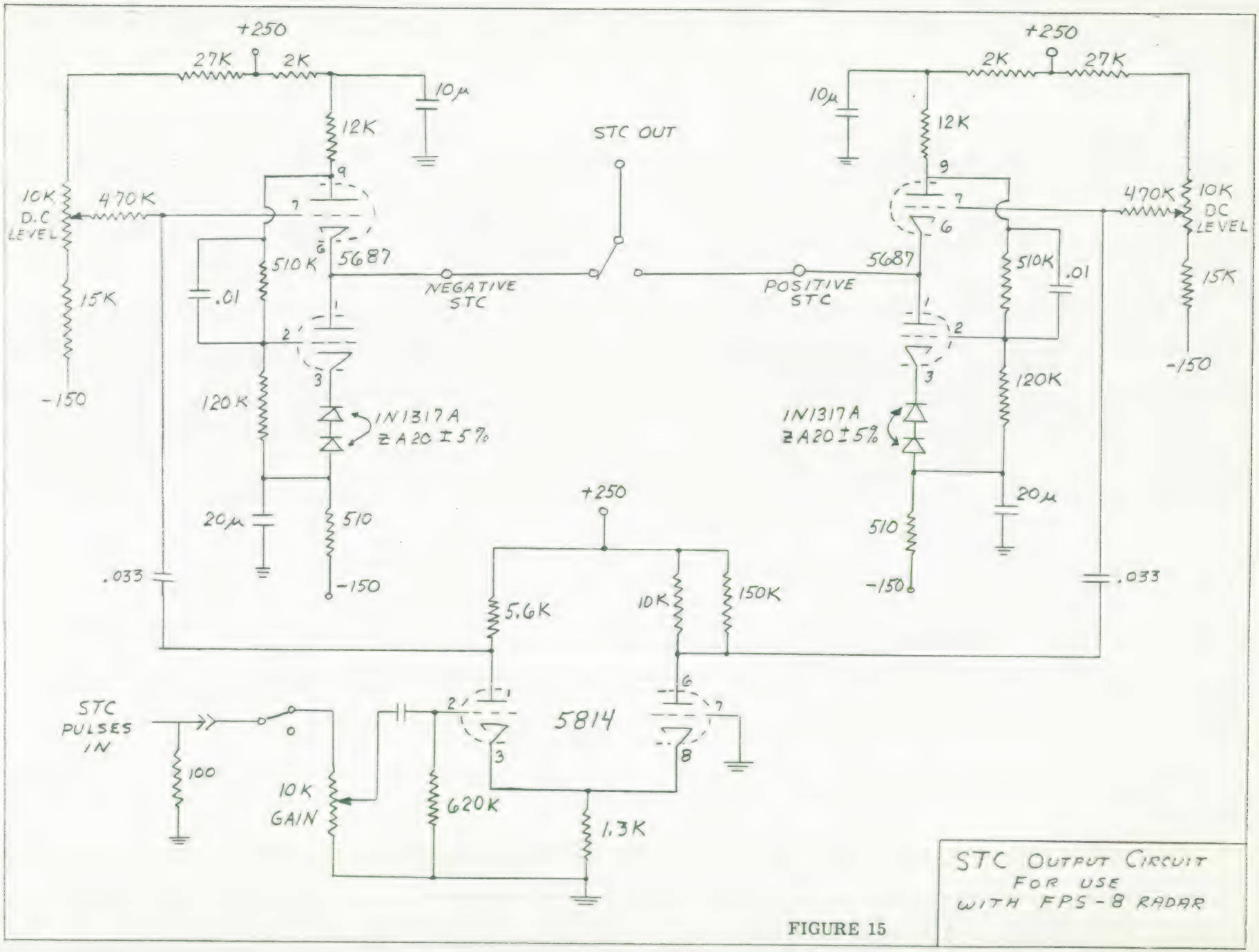
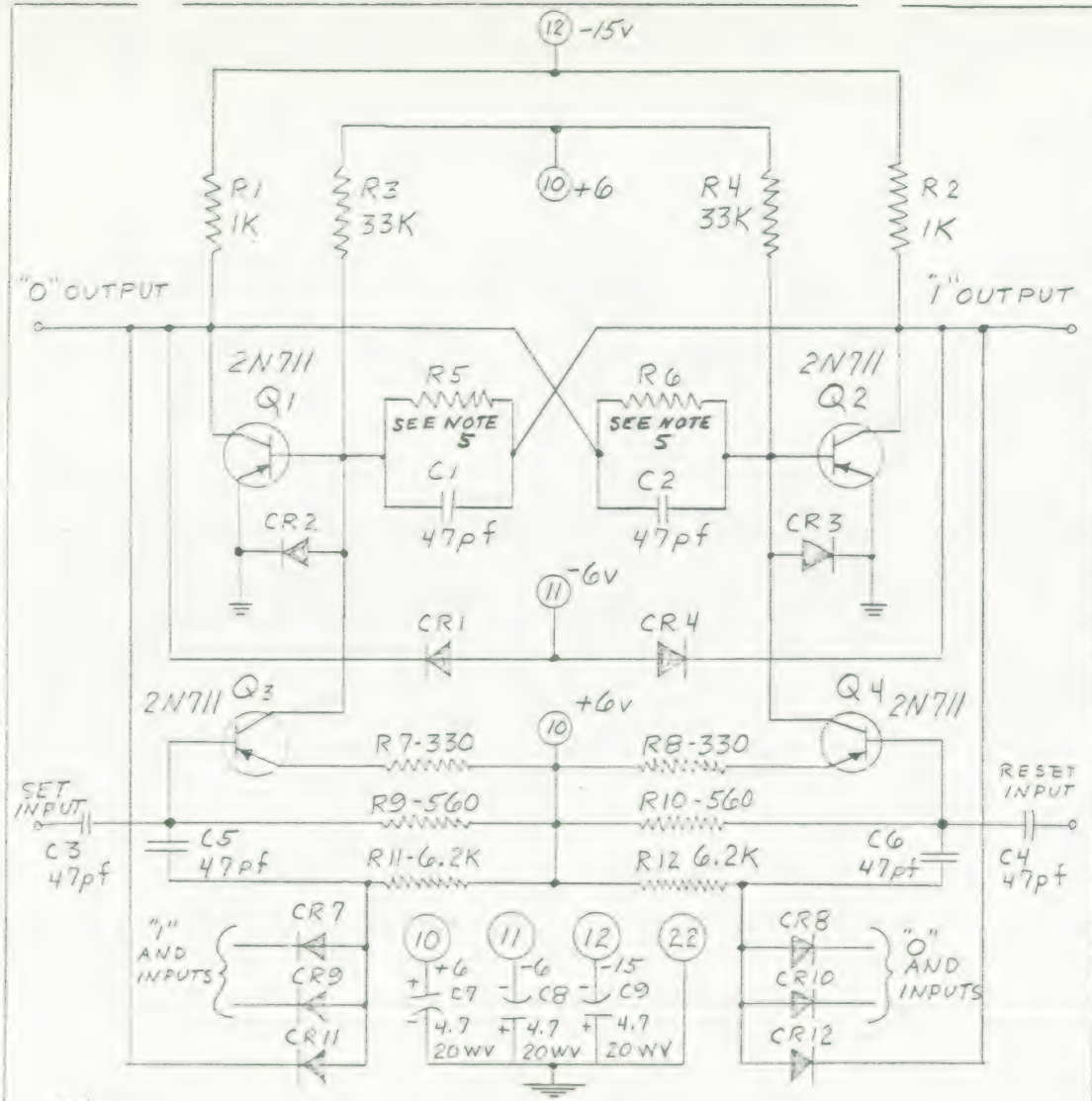


FIGURE 15

STC OUTPUT CIRCUIT
FOR USE
WITH FPS-8 RADAR



FUNCTION TABLE		
PIN#	FFA (3 TO A CARD)	FFB (2 TO A CARD)
1	SPARE	CK#1 "0" OUTPUT
2	CLOCK INPUT	CK#1 "1" AND INPUT
3	CK#1 "1" INPUT	CK#1 SET INPUT
4	RESET INPUT	CK#1 "1" AND INPUT
5	SET INPUT	CK#1 "0" AND INPUT
6	CK#1 "0" INPUT	CK#1 RESET INPUT
7	CK#1 "0" OUTPUT	CK#1 "0" AND INPUT
8	CK#1 "1" OUTPUT	CK#1 "1" OUTPUT
9	SPARE	SPARE
10	+6V DC	+6V DC
11	-6V DC	-6V DC
12	-15V DC	-15V DC
13	SPARE	SPARE
14	CK#2 "1" INPUT	CK#2 "0" OUTPUT
15	CK#2 "0" OUTPUT	CK#2 1" AND INPUT
16	CK#2 "0" INPUT	CK#2 SET INPUT
17	CK#2 "1" OUTPUT	CK#2 "1" AND INPUT
18	CK#3 "1" INPUT	CK#2 "0" AND INPUT
19	CK#3 "0" OUTPUT	CK#2 RESET INPUT
20	CK#3 "0" INPUT	CK#2 "0" AND INPUT
21	CK#3 "1" OUTPUT	CK#2 "1" OUTPUT
22	GROUND	GROUND

CARD NO. & TYPE

A
3-3 THRU 3-24
4-3 THRU 4-23
5-3 THRU 5-24
6-3 THRU 6-23
7-2, 6, 7, 8, 10, 12 THRU 17, 19 THRU 22

B
1-8, 9, 10, 11, 13, 14, 15, 17, 19 THRU 22
2-3, 6, 9 THRU 17, 20, 21, 23
7-1

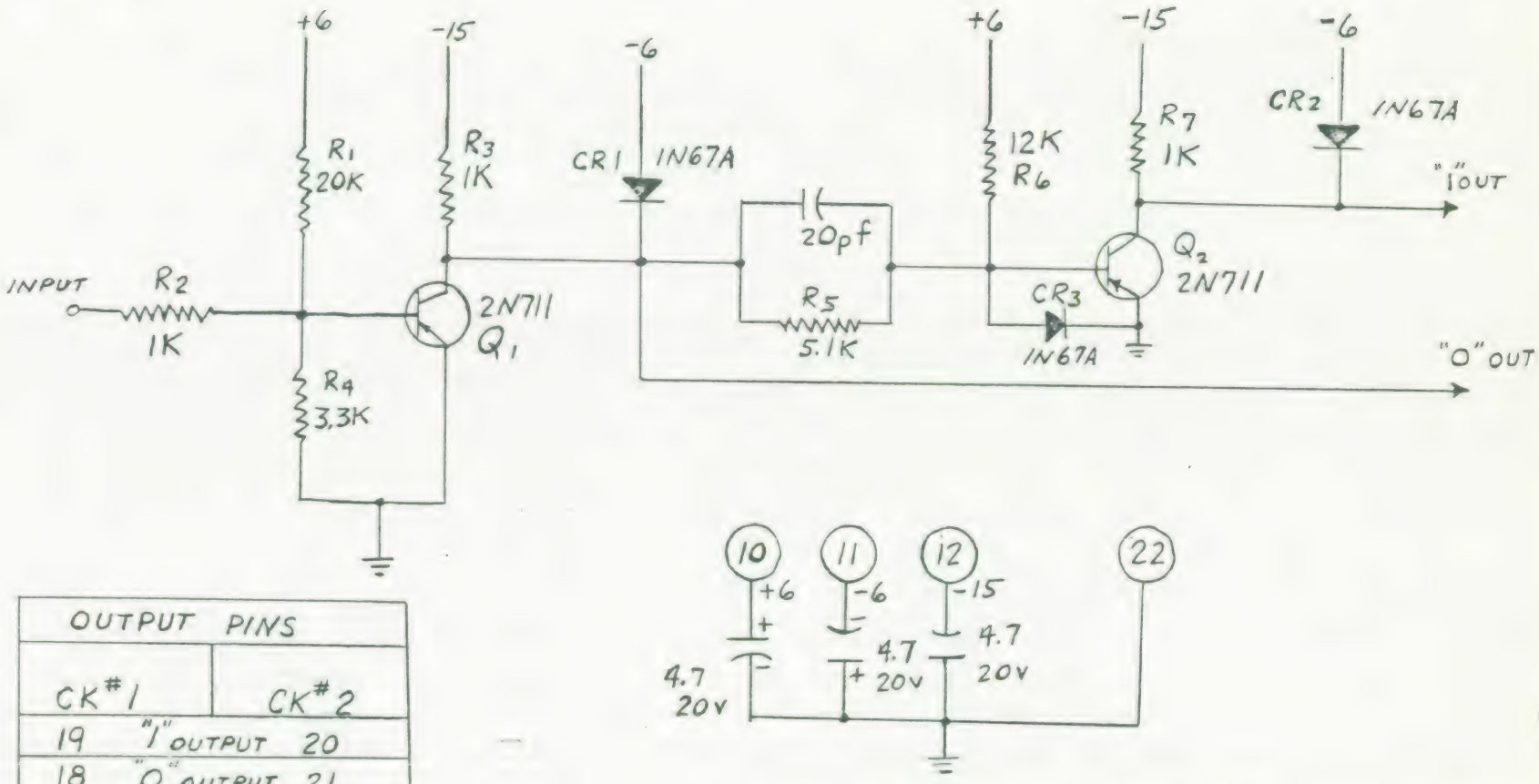
A TOTAL 101
B TOTAL 27

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/2 W ± IN OHMS
2. ALL DIODES ARE IN67A
3. ALL CAP. ARE 1KWVDC IN μf UNLESS OTHERWISE SPECIFIED
4. SEE FUNCTION TABLE FOR PIN CONNECTIONS WITH 2 OR 3 CIRCUITS PER CARD
5. R5 AND R6 ARE 7.5K ON FFA AND ARE 5.1 ON FFB

HIGH SPEED FLIP FLOPS TYPE A AND B

FIGURE 16



OUTPUT PINS	
CK# 1	CK# 2
19 "1" OUTPUT	20
18 "0" OUTPUT	21

1. ALL RESISTORS ARE 1/2 W 5% SHOWN IN OHMS
2. UNLESS SPECIFIED ALL CAP. ARE GIVEN IN μf
3. LOAD RES. FOR AND/OR CIRCUIT 6.2K
4. TWO CIRCUITS PER CARD

FIGURE 17 :
MATRIX SLICER
STC

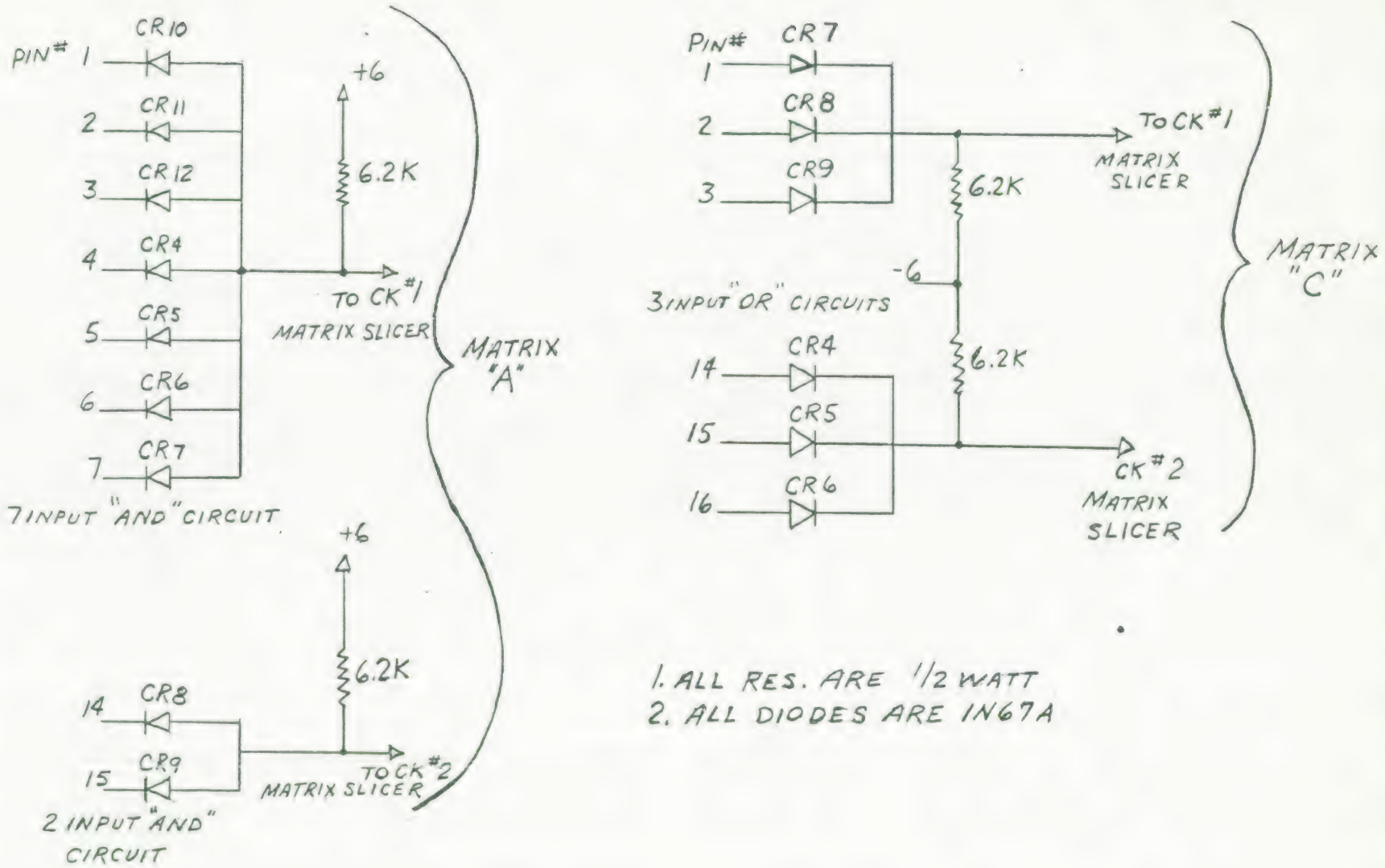
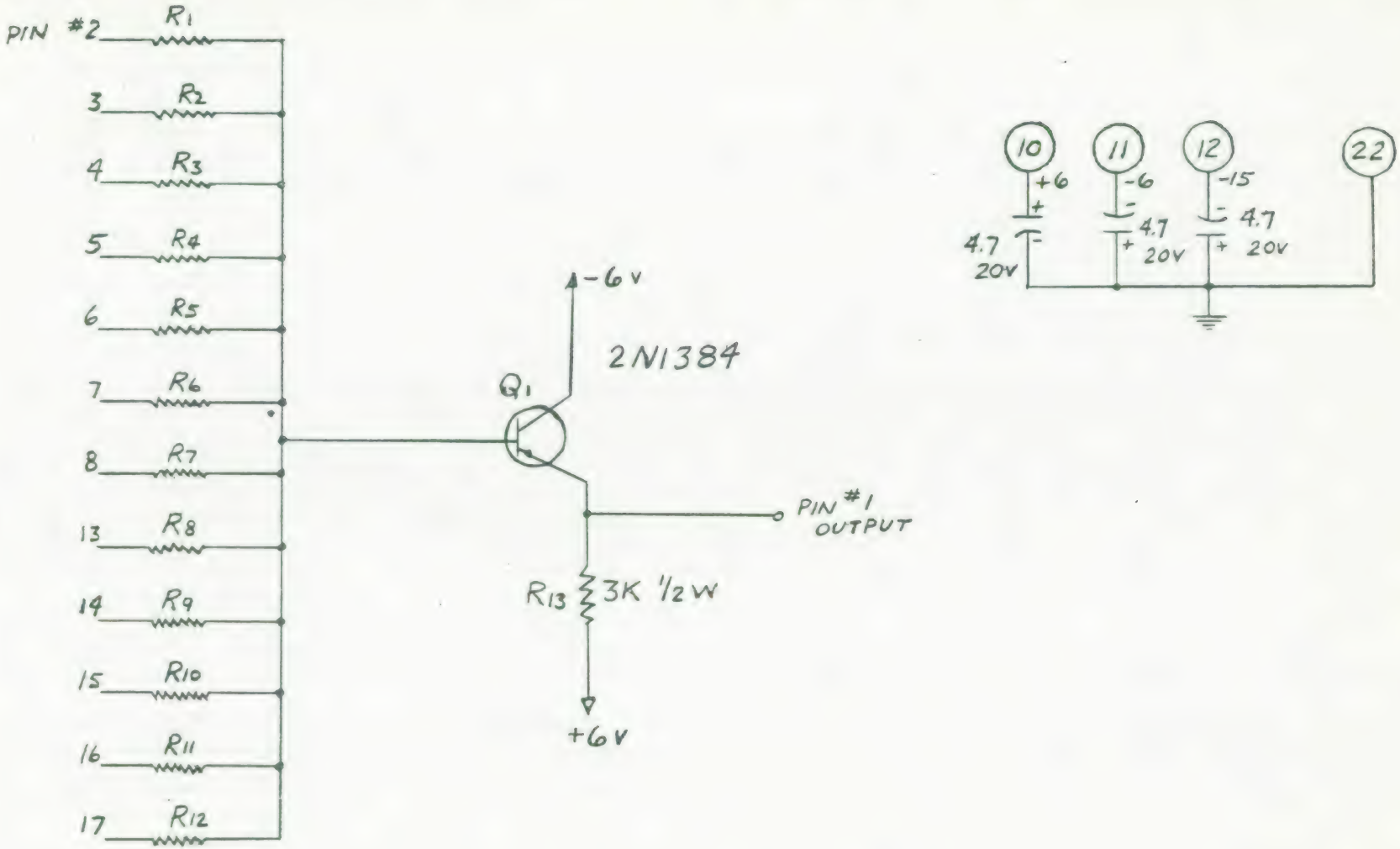


FIGURE 18: MATRIX INPUT CIRCUITS



NOTES: 1. R1 thru R12 are 4.5K, 1%, ½ Watt Resistors.
2. This circuit is built on a Slicer "B" Card.

FIGURE 19: ADDER AND EMITTER FOLLOWER CIRCUIT

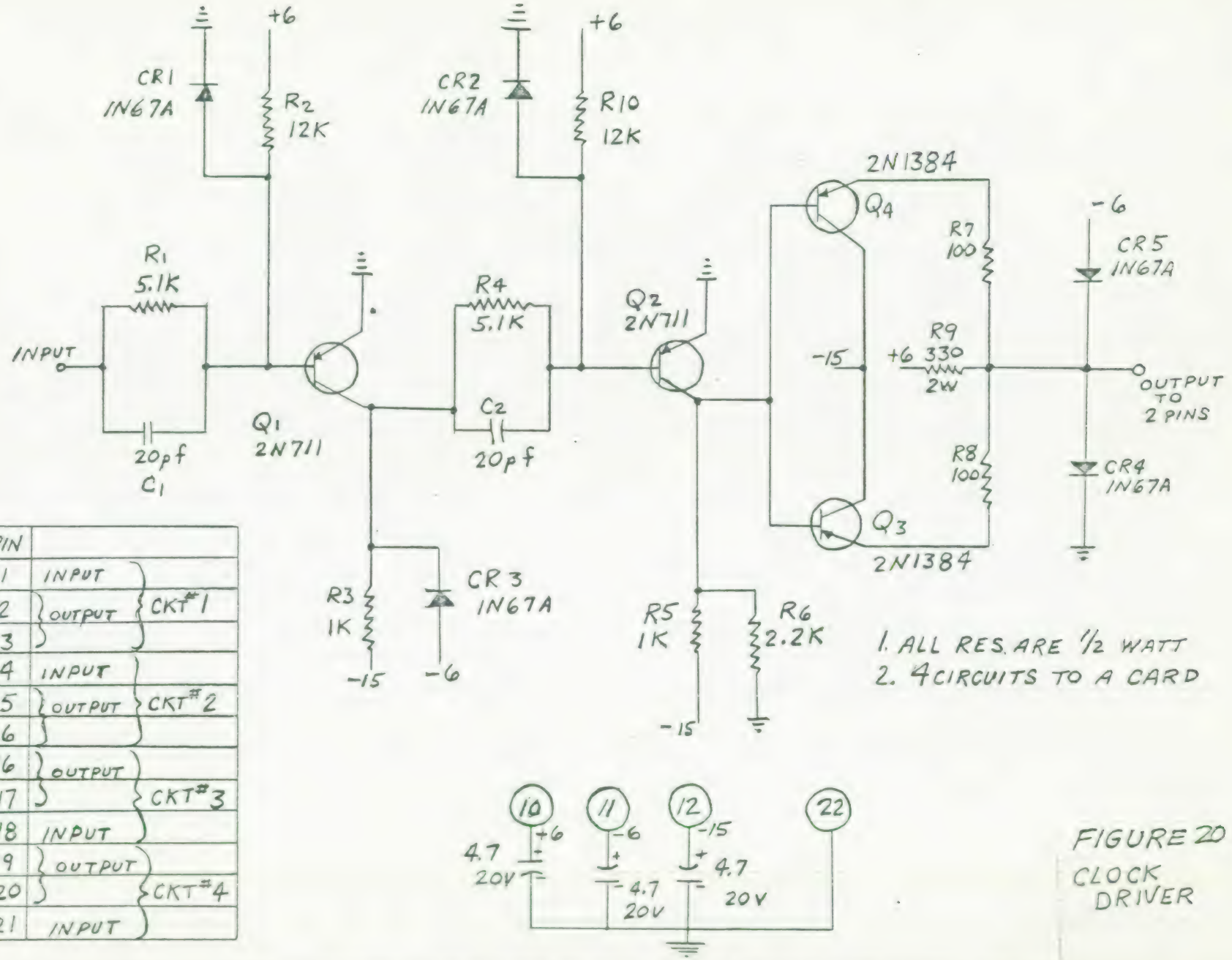


FIGURE 20:
CLOCK
DRIVER

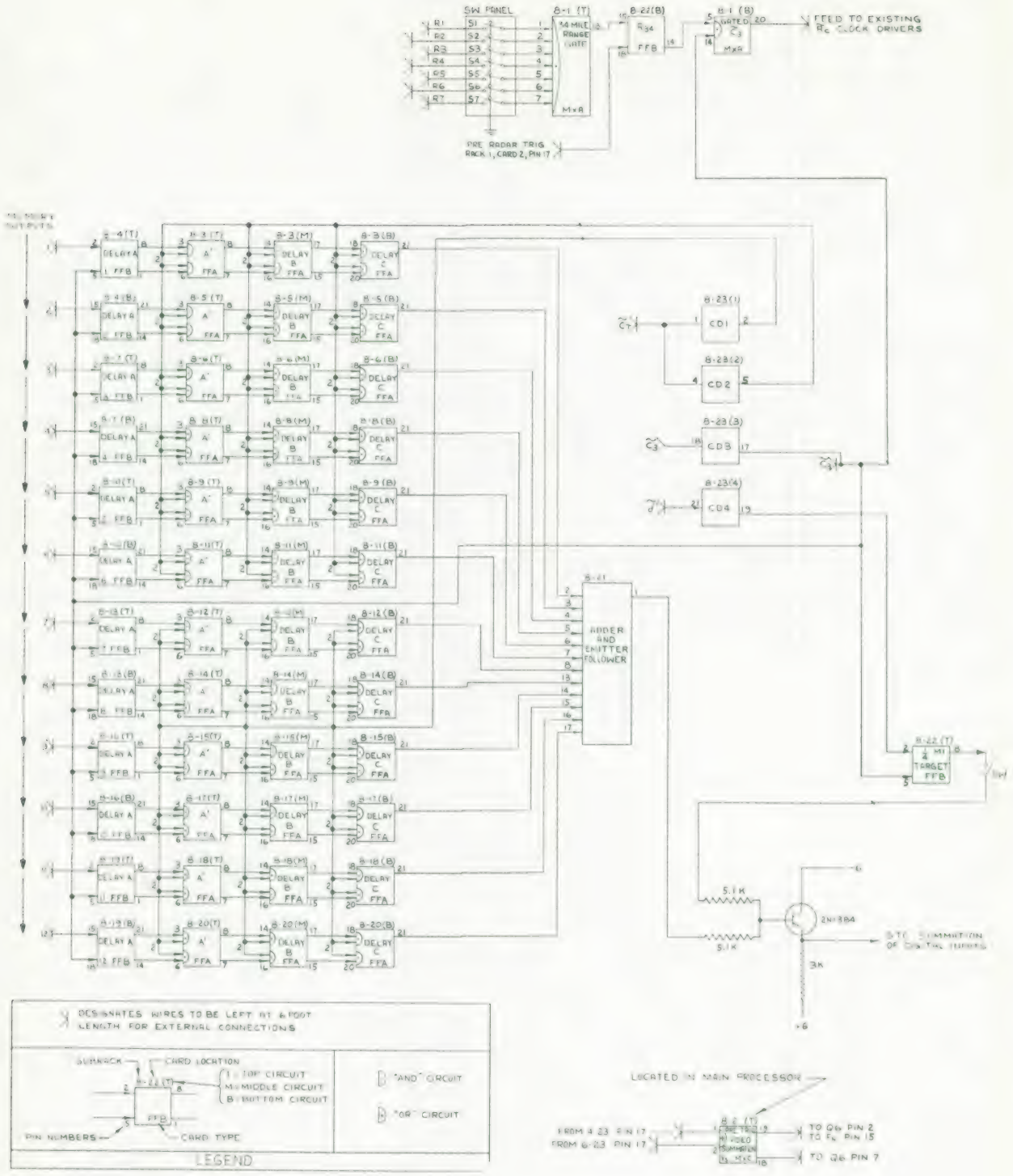


FIGURE 21: SUBRACK 8 - DIGITAL STC

R_1, R_2, R_3, etc., are range gates from the processor, the first being one-half mile long, the second one mile, etc., out to 32 miles in duration. By proper combination of inputs R_1, R_2, etc., a gate of 34 miles is set up. Since R_{34} sets up the length of time C_3 (quarter mile clock pulses) will be allowed to pass, the pre-trigger resets the R_{34} flip-flop to permit C_3 to start again two miles before the next radar sweep. The first C_3 pulse is one-fourth mile after the trigger. This means there is one and three-fourths mile delay left to account for.

3. The quarter mile quantized video is fed into flip-flops Q_{3A} and Q_{3B} along with T_1, T_1', and C_3. The outputs of Q_{3A} and Q_{3B} are fed into their respective 128 series shift registers. The two outputs of the registers are summed so that each radar sweep is again represented as a single video chain.

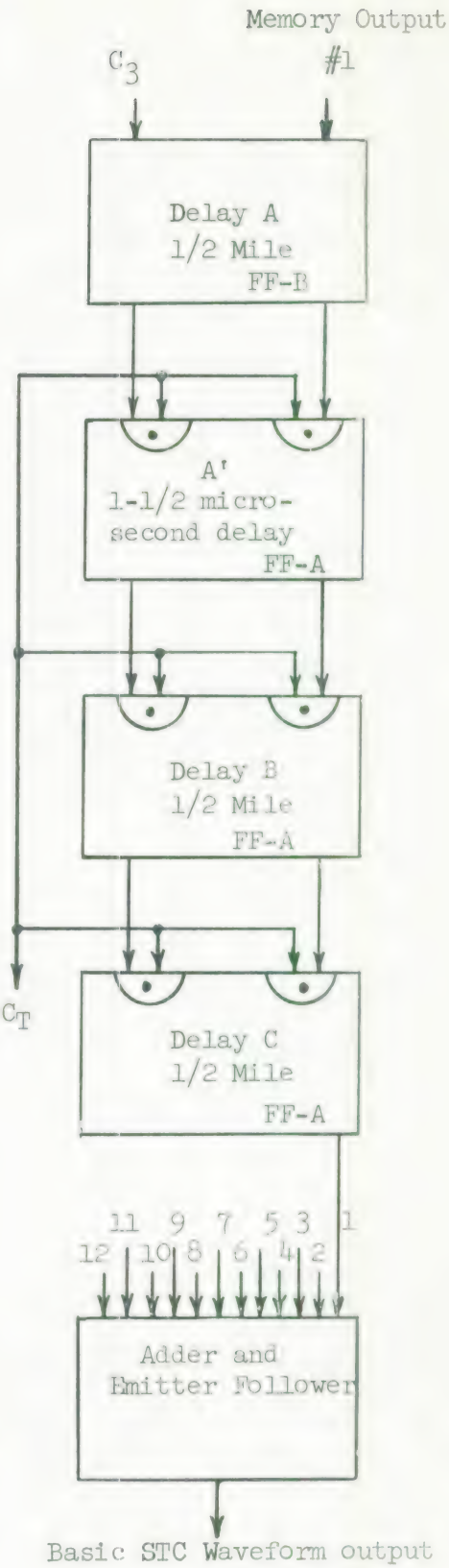
   The output of the video summation is fed to the flip-flops which precede the memory unit in the processor. This information appears to the memory just as it did before, only it is now one and one-half miles early, due to another quarter mile loss in the flip-flop Q_6. This is now the length of time lost in the Automatic Mapper, thereby causing the processed video to start at zero time.

4. Since there is not a prime output on the Memory Unit, a flip-flop (delay A 1/2 mile clocked by C_3) is used to make sure every pulse is represented. If this was not done and C_4 (1/2 mile clock pulses) were used, then every other pulse would be lost.

5. Block A' converts the information to 1/2 mile long pulses. C_T (automatic mapper clocking pulses) is used to pick up a 1-1/2 microsecond delay occurring when converting to C_T clocking after the emitter follower in the processor.

6. Delays B and C each delay the information 1/2 mile giving a total delay of slightly over 1-1/2 miles.

7. Twelve of the above set of circuits are used; one on each of the memory outputs to be fed to the adder. The outputs of these twelve circuits are summed and fed through an emitter follower to form the basic STC waveform (see Figure 14, Page 30).



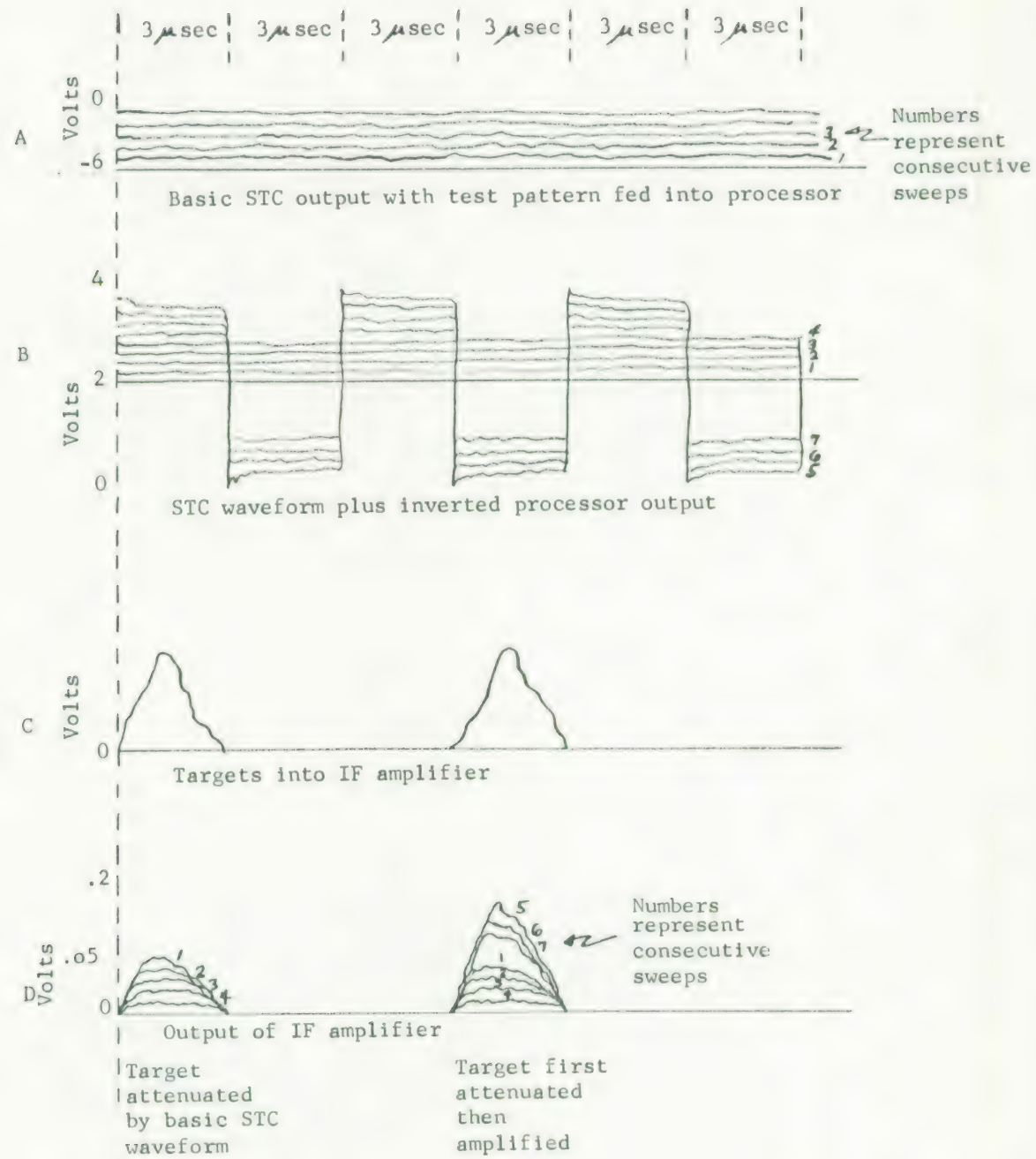


FIGURE 22: DIGITAL STC WAVEFORMS

8. The targets from the processor are pulses 1.8 microseconds long which are permitted to appear during the proper one-fourth mile interval. This process does not indicate the location of the aircraft within the one-fourth mile increment. The targets, therefore, must be lengthened to one-fourth mile when used as a bias voltage to ensure an effect on the aircraft return. Since this system uses trailing edge logic, the prime side of the processor output can be fed to a flip-flop and clocked with C_3, thereby increasing the targets to one-fourth mile duration.

9. The summation of the output of the STC circuit and the lengthened processor targets is combined with a DC level control. This level control is similar to the one used in the previously mentioned analog circuits. The STC output circuit is shown in Figure 15, Page 32.

The following circuits shown on Pages 33 - 38 include the individual solid-state circuits used in the digital STC voltage waveforms generator.

Figure 16 - Flip-flop circuit used. These are packaged 2 or 3 to a card depending on the number of inputs needed. The function table shows the pin connections for both types of flip-flop cards.

Figure 17 - This is the standard matrix slicer, two of which are on each matrix card. A variety of input circuits can be used with them.

Figure 18 - Shows the input circuits used on the matrix cards for the STC circuitry.

Figure 19 - This is the adder and emitter follower circuit used to sum the twelve memory outputs.

Figure 20 - The clock driver circuits are used as isolation amplifiers.

Figure 21 - This is the complete logic block diagram for the circuitry used in conjunction with the processor.

D. RESULTS AND EVALUATION

The AN/FPS-8 radar, on which this unit was tested, has an I-F amplifier in the MTI receiver which limits only very strong signals. The output of the phase detector is then a function of not only the phase relationship between I-F video and the coho signal, but also the amplitude of the I-F amplifier output. Since the above is true, a gain controlling device, such as this digital STC unit should be able to regulate the video levels.

When the processor had been modified for use as a STC unit, several tests were conducted to observe: (1) whether the unit functioned as designed and (2) the effect of this type of gain controlling device on the I-F amplifier. Upon checking out the digital STC unit, it was evident that stray pulses were being picked up within the unit. The new subrack, containing the additional logic circuits, had all inter-connecting wires cabled together to tie into the processor. Within this bundle of wires, pulses were picked up between various leads, thereby causing many undesirable effects in the unit. This was easily corrected by rearranging the leads.

The unit was designed to utilize a pretrigger; however, one was not used for testing at the present time. Data for 34 miles was fed into a register with only a sufficient number of bits to store 32 miles of information in 1/4 mile increments; the first two miles of data being dumped out and lost. This data could have been preserved with a pretrigger, but for our purpose, this was not necessary. The unit provided pulses which coincided with incoming video indicating

the timing and delay circuitry was functioning properly.

Since the unit was to be used in conjunction with the AN/FPS-8, its I-F amplifier was removed and connected to the STC unit under simulated conditions. The effect of pulses from the STC unit on a simulated target in the I-F strip was observed (see Figure 22, Page 41). While the STC DC level could be shifted from 0 to 3 volts, the best operating condition occurred at 2 volts with a bias controlling waveform set not to exceed a maximum excursion of $\pm$ 1 volt. A positive STC pulse reduced signals from 0.05 volt to 0.005 volt.

Increasing the STC bias voltage to a new maximum resulted in attenuating the IF signal faster (i.e., in fewer sweeps). This, however, does not utilize the number of voltage increments provided by the unit. This range of STC voltage is, as was expected, the same as the range of control used previously with the logarithmic unit. A negative pulse applied to the cathode resulted in signal amplification from a 0.05 volt level to a 0.2 volt level. Of course, once the signal was amplified to the point of limiting, further negative biasing only distorted the signal waveform. During this time, it was noted that the STC pulses were not distorted, nor do they appear at the I-F amplifier output.

Since the unit proved to be capable of providing the gain control in any one-half mile increment under the above conditions, the I-F amplifier was returned to its location in the radar. With the digital STC unit located 800 feet from the radar, the time lost in transmitting the video to the processor and returning the STC gain control function back to the radar was easily overcome by advancing the STC output. This was accomplished by initiating the clock pulse train which controls

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the series shift storage registers by an equal period earlier in time. The gate length could only be adjusted in 6 microseconds increments; hence, the minimum difference in time between a video pulse and its subsequent counterpart from the STC unit was approximately 2 microseconds.

The STC output circuits shown in Figure 15, Page 32, was located in the radar tower. This circuit amplified the pulses, permitted adjustment of the DC level, and provided STC waveforms of either polarity. This was done so that, in addition to cathode biasing the MTI I-F amplifier, the unit could be used to control the grid biasing of the normal receiver if desired.

When the unit was first tested with MTI video feeding the processor, and the processor in turn controlling the MTI I-F amplifier, the desired effect was not realized. The STC waveform appeared as a baseline distortion all through the MTI receiver with some pulses appearing as an increase in noise and false targets at the output of canceled video.

Four sweeps were required to identify a target. This resulted in the loss of some targets, since by then, the STC had reduced them below the threshold level of the processor. Even excluding the latest four sweeps of information from the STC summation, thereby letting the targets be identified before they were attenuated, did not improve the situation. The idea of increasing the gain during the one-fourth mile interval containing a target was dropped and only the basic STC waveform was used.

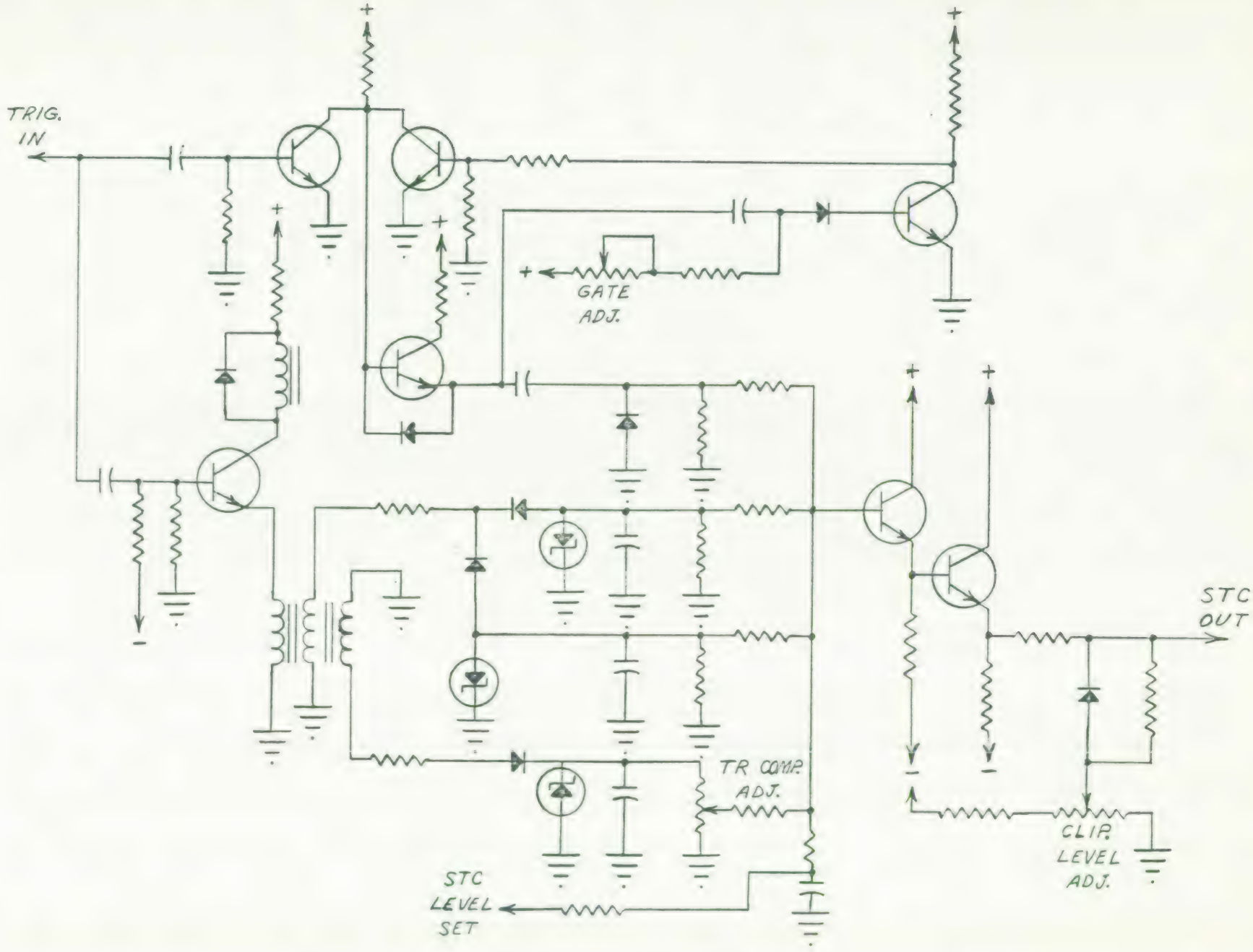


FIGURE 24 TRANSISTORIZED STC CIRCUIT

With just the basic STC waveform used, the MTI output deteriorated and additional uncanceled information was still displayed on the P.P.I. It was first thought that the MTI coherency was upset. Perhaps the pulses were inducing rapid phase shifts in the I-F amplifier thereby causing the phase detector to identify false targets. Also, since the STC pulses could be compared to a square wave, they might have a 30 mc component which would be amplified through the 30 mc bandpass I-F amplifier.

A filter was inserted in the STC line to eliminate frequencies above 10 megacycles. The condition still persisted. Next, the closed loop was opened and test pulses were fed through the processor and simulated 30 mc signals were fed through the MTI system. No apparent phase shift; i.e., disturbance of coherency, could be observed. Whenever the STC pulse was generated from an external source rather than from MTI video, the gain controlling characteristic behaved in the desired manner. When the loop was closed, the basic STC function did surpress clutter, but it did not bring out targets which were within dense clutter. For the processor to work properly, the MTI gain had to be set so high that the scope presentation was poor. The STC unit never returned the presentation to a condition which was comparable to what was considered previously as good MTI.

E. CONCLUSIONS

Since the digital STC unit was separated from the radar by a distance of 800 feet, the timing was not exactly right for coincidence. A less sophisticated unit providing only the STC waveform, not target

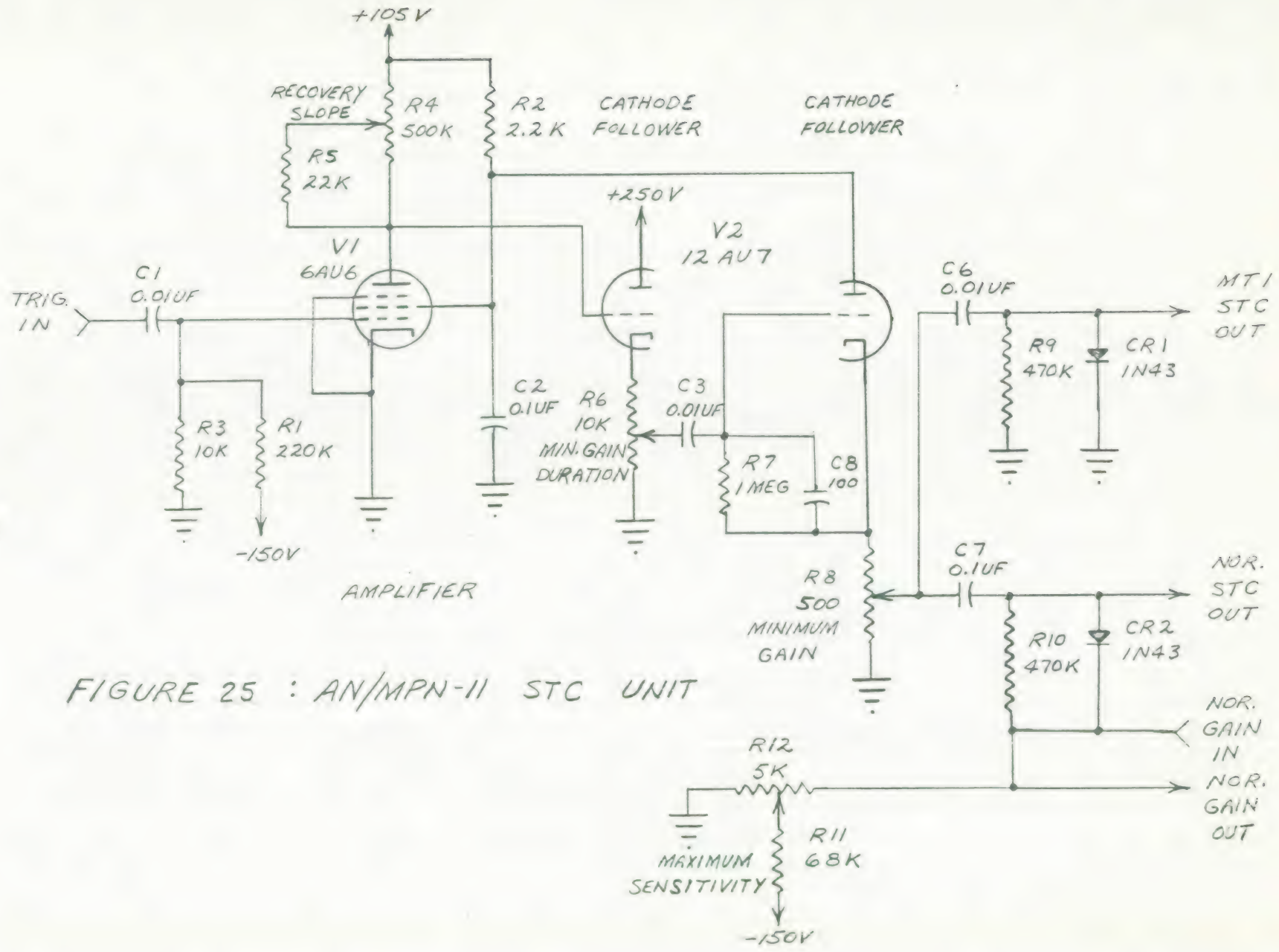
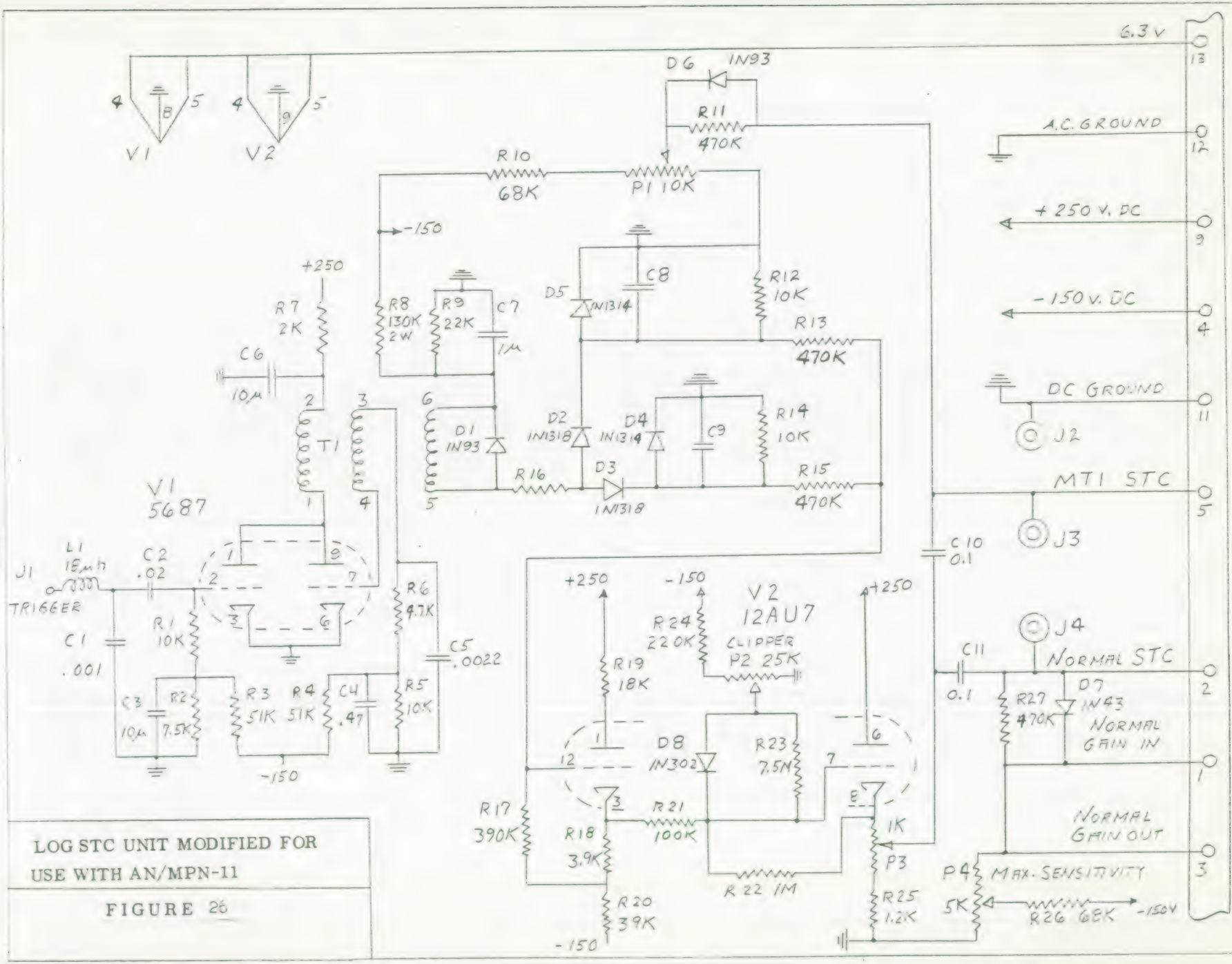
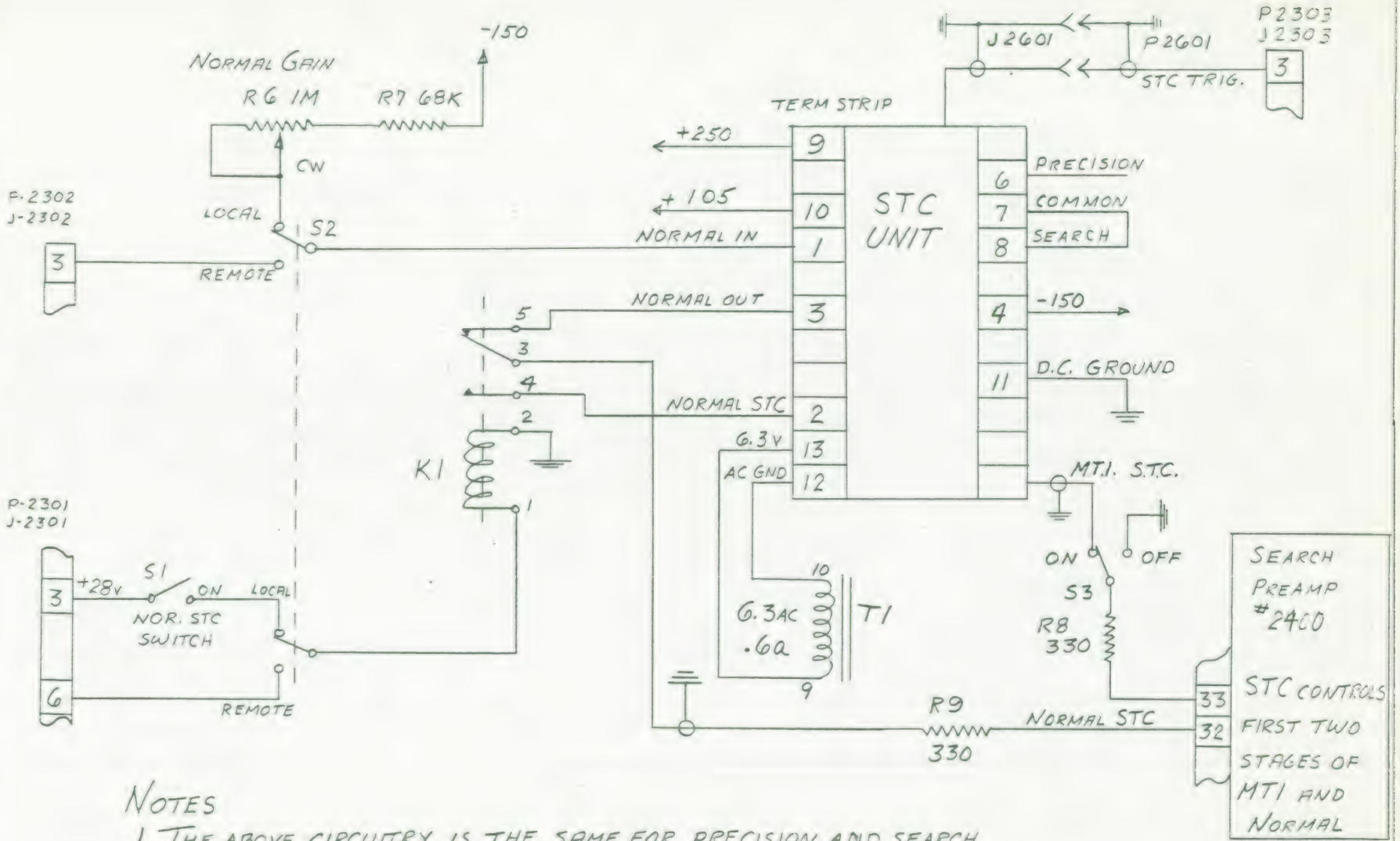


FIGURE 25 : AN/MPN-11 STC UNIT



LOG STC UNIT MODIFIED FOR USE WITH AN/MPN-11

FIGURE 26



NOTES

1. THE ABOVE CIRCUITRY IS THE SAME FOR PRECISION AND SEARCH WITH DIFFERENT NOMENCLATURE. THE SEARCH CIRCUITRY IS SHOWN

CIRCUITRY ASSOCIATED WITH STC UNITS IN THE MPN-11 RADAR

FIGURE 27

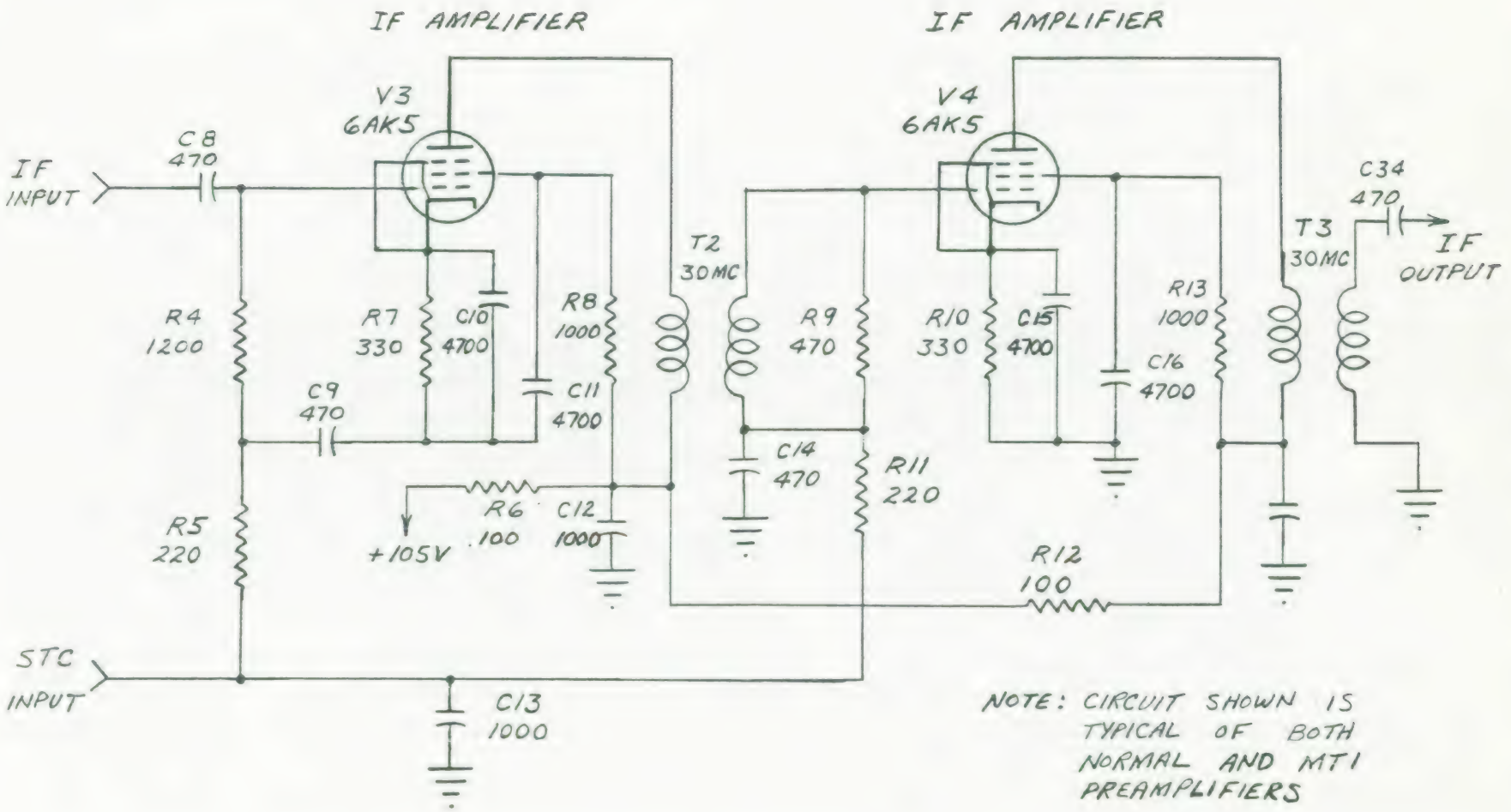


FIGURE 28: AN/MPN-11 PREAMPLIFIER

reinforcement, could prove to be more successful if located in close proximity to the MTI receiver cabinet. The idea of reinforcing the targets does not warrant the additional expense and complexity of circuitry necessary to accomplish this.

A less complicated system could have a smaller memory unit or utilize the extra cells to store one-fourth rather than one-half mile increments. If two registers within the memory unit could be operated by an independent series of clock pulses, they could be used to replace the large number of flip-flops presently used to correct the timing. The auto-map portion and its associated circuitry also would not be necessary. With the advances in the state of the art, such a unit could be packaged in a fraction of the space occupied by the present processor. Further investigation with a unit such as the one described above could eventually provide an optimum STC function.

SECTION 4

RECOMMENDATIONS

A. GENERAL

This report outlines some developmental efforts in the field of clutter attenuating devices for EMS radars. The work reported herein has offered an insight into some specialized problems involving STC and video processing. It has also pointed the way to problem areas where further development is needed. Therefore, the following specific recommendations are presented below and discussed briefly.

B. APPLICATIONS TO PRECISION RADAR, AN/TPN-14

It has been noted that excess ground clutter can occur on the elevation portion of the AN/TPN-14 display, and this may make tracking difficult on a low glide slope approach (2-degree or less). An improved STC unit should be investigated as a possible solution to this problem. Since the AN/TPN-14 does not have MTI, the obvious solution would be to incorporate MTI to eliminate ground clutter. However, experience has shown that GCA controllers prefer normal video for display so as not to lose the returns from the runway markers. Addition of an MTI receiver would necessarily add to the size, weight, alignment and maintenance considerations which are vitally important in an EMS radar. It is felt that an improved STC unit, similar to the logarithmic one discussed in Section 2, could be developed to effect a satisfactory solution to this problem with no increase in size or weight. Alignment and maintenance would be comparable to that

required by the STC unit presently used in the AN/TPN-14.

C. FUTURE DIGITAL APPLICATIONS

The end result of what this report hoped to accomplish was a more positive identification of targets (i.e., better isolation from noise, clutter, etc.) so as to provide a cleaner PPI presentation for an operator and better video for automatic tracking circuits. The Video Digital Processor used in this study did a good job identifying targets by means of a statistical analysis of the video history for the preceding 16 range sweeps. The use of a linear amplifier in the radar receiver could further enhance the capability of this unit by eliminating the saturation effect in the present limiting IF amplifier. In addition, there is no means provided to remember whether a target had been identified during the previous azimuth scan so that the criteria for continued identification might be improved, or targets which have not moved could be eliminated.

This could easily be done by using a drum memory whose rotation is synchronized with the radar antenna (see Figure 23, Page 46). With an antenna rotation of 10 RPM, there would be 6 seconds between consecutive radar contacts with the aircraft. To have the aircraft detected by the processor and drum, the aircraft would have to move 1/4 mile in a radial direction in 6 seconds.

$$\frac{.25 \text{ nautical mile}}{6 \text{ sec.}} = 150 \text{ knots}$$

Aircraft flying with a radial speed greater than 150 knots could easily be detected using 1/4 mile resolution in the system. Commercial memories are available with core memories which operate in less than 3 microseconds.

Another way in which a drum memory might be utilized is to have it retain a DC level in each 1/4 mile increment as a function of the IF amplifier output amplitude occurring that instant. During the next azimuth sweep, the memory would be generated from its output, then the memory would be updated with the present video. Since a target would be moving and would not re-occur in the same increment, it would not tend to attenuate itself.

D. TRANSISTORIZED LOG STC

The STC unit is a small part of the complete radar set; therefore, it is not practical to transistorize the STC unit alone. The present state of the art, however, does not preclude the development of a transistorized radar receiver which would also meet the required environmental specifications. In fact, development work is currently in process on solid-state radar recievers. For this reason, it was felt that the possibility of reducing the logarithmic STC unit dicussed in SECTION 2 to a solid-state module should be investigated. A considerable reduction in size, weight and power requirements can be realized by use of the circuit shown in Figure 24. The circuit as shown was not breadboarded; hence, values are not specified. A small amount of additional effort would yield a miniaturized STC module suitable for use with any solid-state radar receiver.

E. AN/MPN-11 STC IMPROVEMENTS

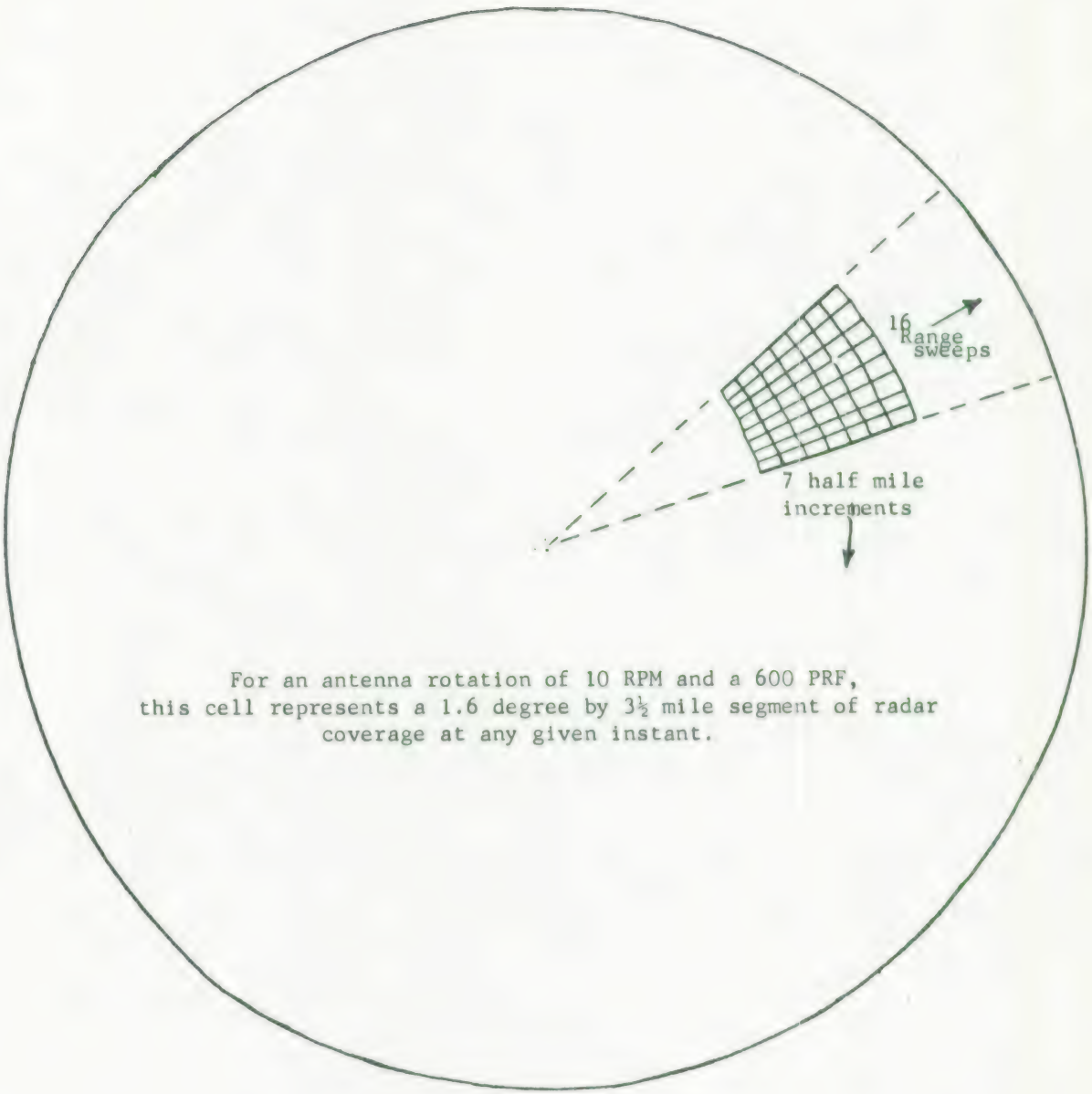
As an example of how the logarithmic STC unit can be adapted to use in other radars, a unit was breadboarded for the AN/MPN-11. The AN/MPN-11 radar set is a complete ground controlled approach (GCA) facility with the capabilities to serve as an air traffic control center. The entire system is packaged in two trailers and contains three major sub-systems; a search radar system for locating aircraft within a 40-mile radius; a precision radar system for tracking aircraft during the final approach; and radio communication equipment for ground-to-aircraft communication.

A logarithmic STC unit was designed to replace the existing circuit (Figure 25) without having to modify the radar set. A schematic of the new circuit is shown in Figure 26 and is designed to utilize existing pin numbers in the same function as they were previously used. Figure 27 shows the existing associated AN/MPN-11 circuitry used in conjunction with the STC unit.

The AN/MPN-11 STC unit provides grid biasing for both the Normal and MTI preamps (Figure 28). With the new unit, the DC levels of the STC waveform can be set independently, the Normal by its existing gain control, and the MTI by the new potentiometer P1. Two function generators are provided which permit the summation of a short and a long R-C time constant. The selection of C8 and C9 will be determined by the slope of the waveform necessary to match the characteristic of the preamp so as to provide the 12 db octave gain characteristic desired. This same circuitry is duplicated for both the search and precision sections of the radar.

A P P E N D I X I

SUPPLEMENTARY REPORT ON THE SOLID STATE DIGITAL VIDEO PROCESSOR



Pictorial representation of Sampling Cell

FIGURE 29

A P P E N D I X I

OBJECT

The object of this Appendix is to serve as a supplement to the Rescon Video Digital Processor Final Report so that it may be more easily understood and maintained. Drawings and schematics for the unit were never delivered because the Rescon Corporation went out of business. A complete set of schematics for the printed circuit boards can be found at the end of this Appendix.

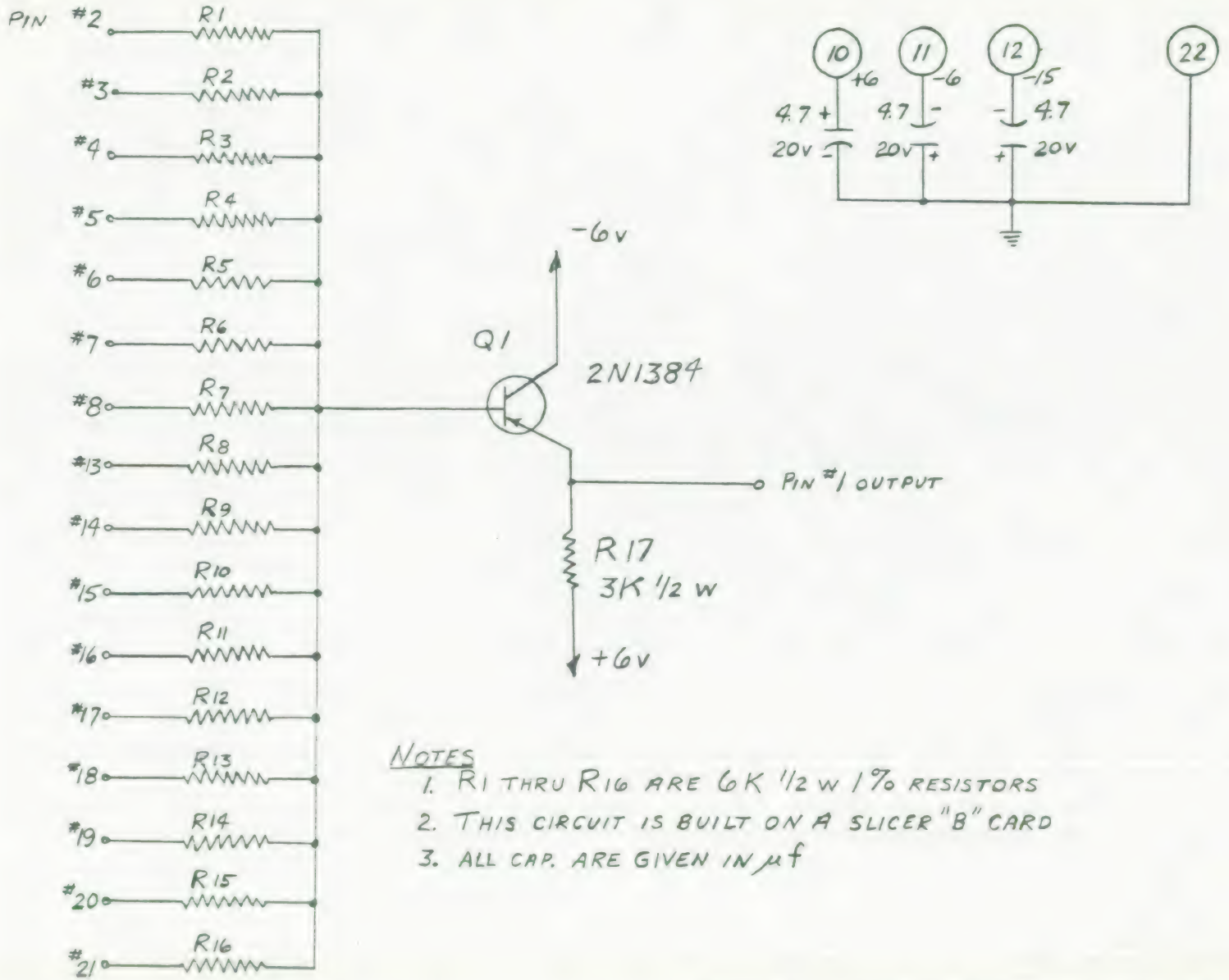
G E N E R A L I N F O R M A T I O N

This unit was built by Rescon and delivered to Fort Dawes on 21 August 1961. It was initially tested by Rescon personnel from September to November of that year and, during that time, the following problems occurred.

1. Some stray pulses were being picked up through the inter-chassis cabling. This was corrected by regrouping some of the wires so that those carrying conflicting pulses were not adjacent to one another.
2. Criteria for establishing a target was changed from 6/16 to 8/16 hits, and for continuance of a target from 4/16 to 6/16 hits. This eliminated some false targets out of the Processor due to the criteria being set too low. To accomplish this, the inputs to A1 and A2 were changed from D6, D8, and D10 to D6, D8, D10, and D12.
3. If two or more consecutive bits of information entered Q6, every other one was prevented from passing through. By feeding the Q5 prime output into the prime "and" input of

Q6, it then enables the flip-flop to remain in the "1" position for two consecutive half mile pulses, rather than resetting to the "0" position.

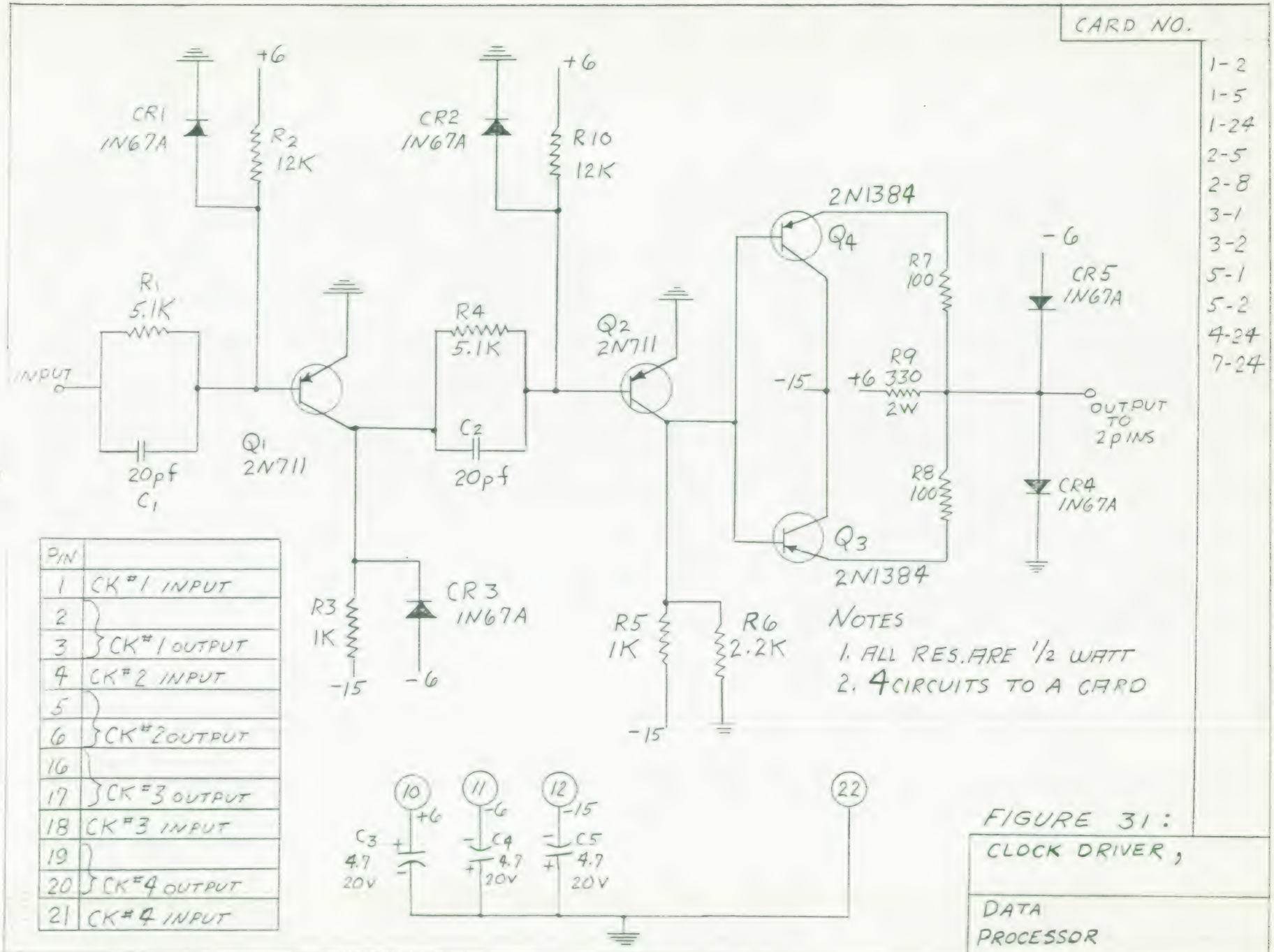
4. D4A, D6A, etc. only permitted every other bit of information to feed through the first stage flip-flop if two or more consecutive bits entered the shift register. This was corrected by adding to the prime input "an" circuit, the prime output of its respective slicer.
5. The same problem occurred with D4B, D6B, etc., and was corrected in the manner described in Paragraph 4.
6. The automatic clip level control originally had a time constant of 17 seconds. This meant that, as the machine sampled the input noise level, it took 17 seconds to adjust its input voltage sensitivity to an optimum level for inhibiting the passage of input noise. This optimum level is predetermined by the operator. The time constant was changed to 2.5 seconds to allow a more rapid adjustment. This was accomplished as follows:
   a) Change the 200 microfarad capacitor at the input of Q3 to 50 microfarads.
   b) Change the 350 microfarad capacitor at the circuit output to 50 microfarads.
7. The adder circuit which feeds slicers B and C are not isolated from the slicer inputs. This meant that the slicer input circuit was also providing a DC level to the summation point.



NOTES

1. R1 THRU R16 ARE 6K 1/2 w 1% RESISTORS
2. THIS CIRCUIT IS BUILT ON A SLICER "B" CARD
3. ALL CAP. ARE GIVEN IN μf

FIGURE 30: ADDER AND EMITTER FOLLOWER, DATA PROCESSOR



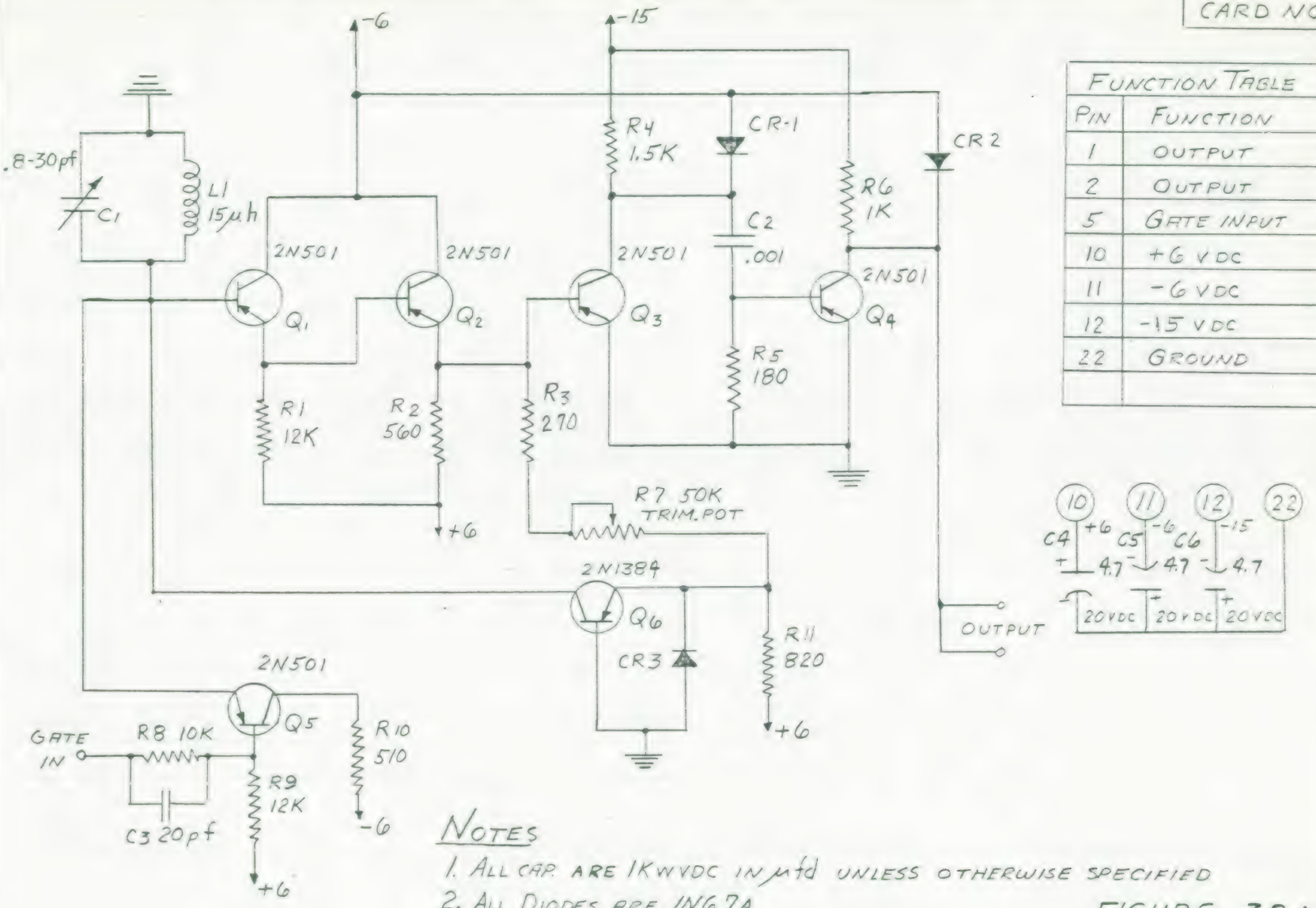
PIN	
1	CK#1 INPUT
2	} CK#1 OUTPUT
3	
4	CK#2 INPUT
5	} CK#2 OUTPUT
6	
16	} CK#3 OUTPUT
17	
18	CK#3 INPUT
19	} CK#4 OUTPUT
20	
21	CK#4 INPUT

NOTES
1. ALL RES. ARE 1/2 WATT
2. 4 CIRCUITS TO A CARD

FIGURE 31:
CLOCK DRIVER,
DATA PROCESSOR

CARD NO. 2-4

FUNCTION TABLE	
PIN	FUNCTION
1	OUTPUT
2	OUTPUT
5	GATE INPUT
10	+6 V DC
11	-6 V DC
12	-15 V DC
22	GROUND



NOTES

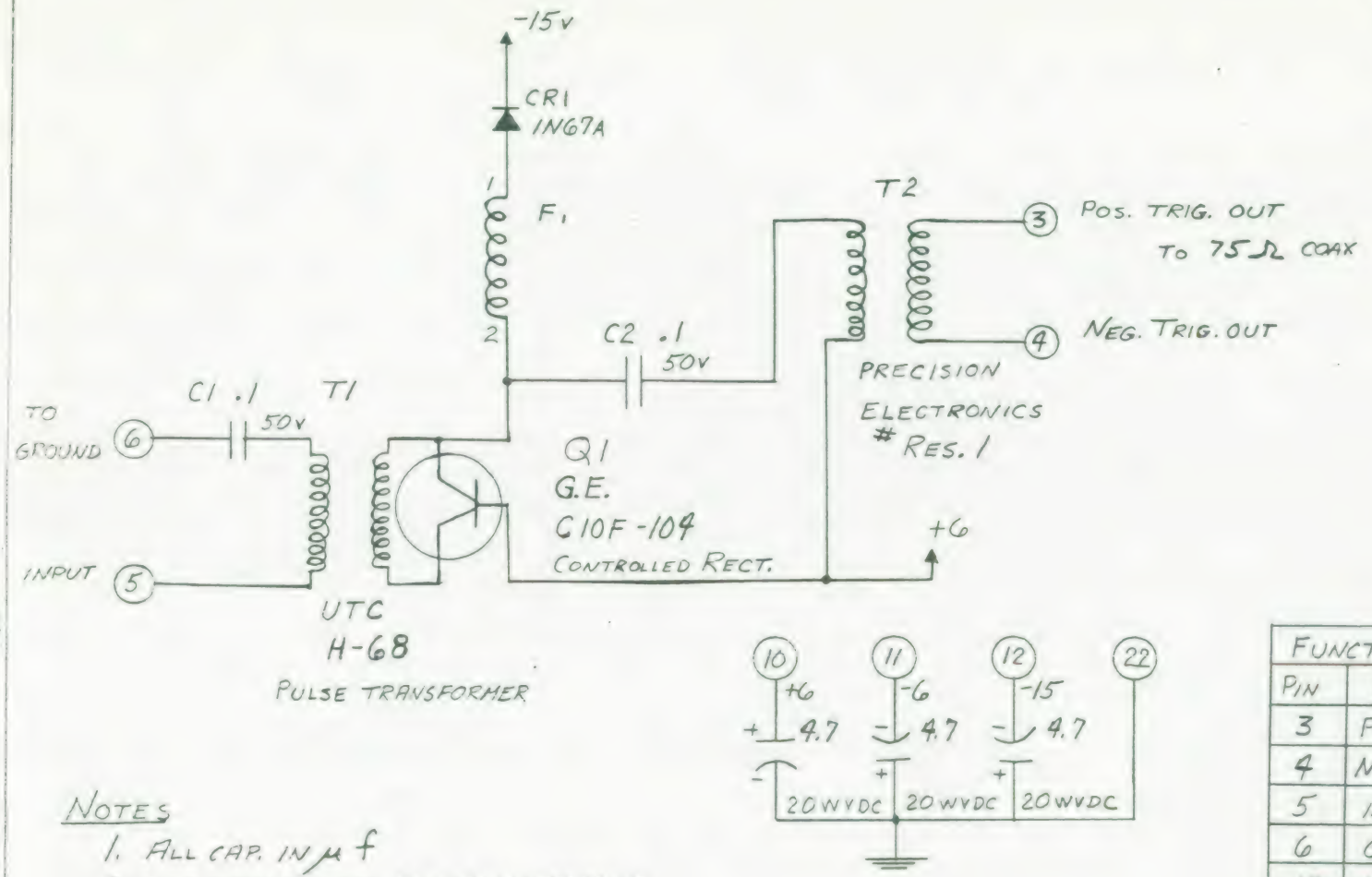
1. ALL CAP. ARE 1KWVDC IN μfd UNLESS OTHERWISE SPECIFIED
2. ALL DIODES ARE 1N67A
3. ALL RESISTORS ARE GIVEN IN OHMS, ½ WATT ±5% UNLESS OTHERWISE SPECIFIED
4. SEE TABLE FOR PIN CONNECTIONS
5. 15μh CHOKE = WILCO No. 1015-15

FIGURE 32:

GATED CLOCK OSCILLATOR,

DATA PROCESSOR

CARD No. 4-1



NOTES

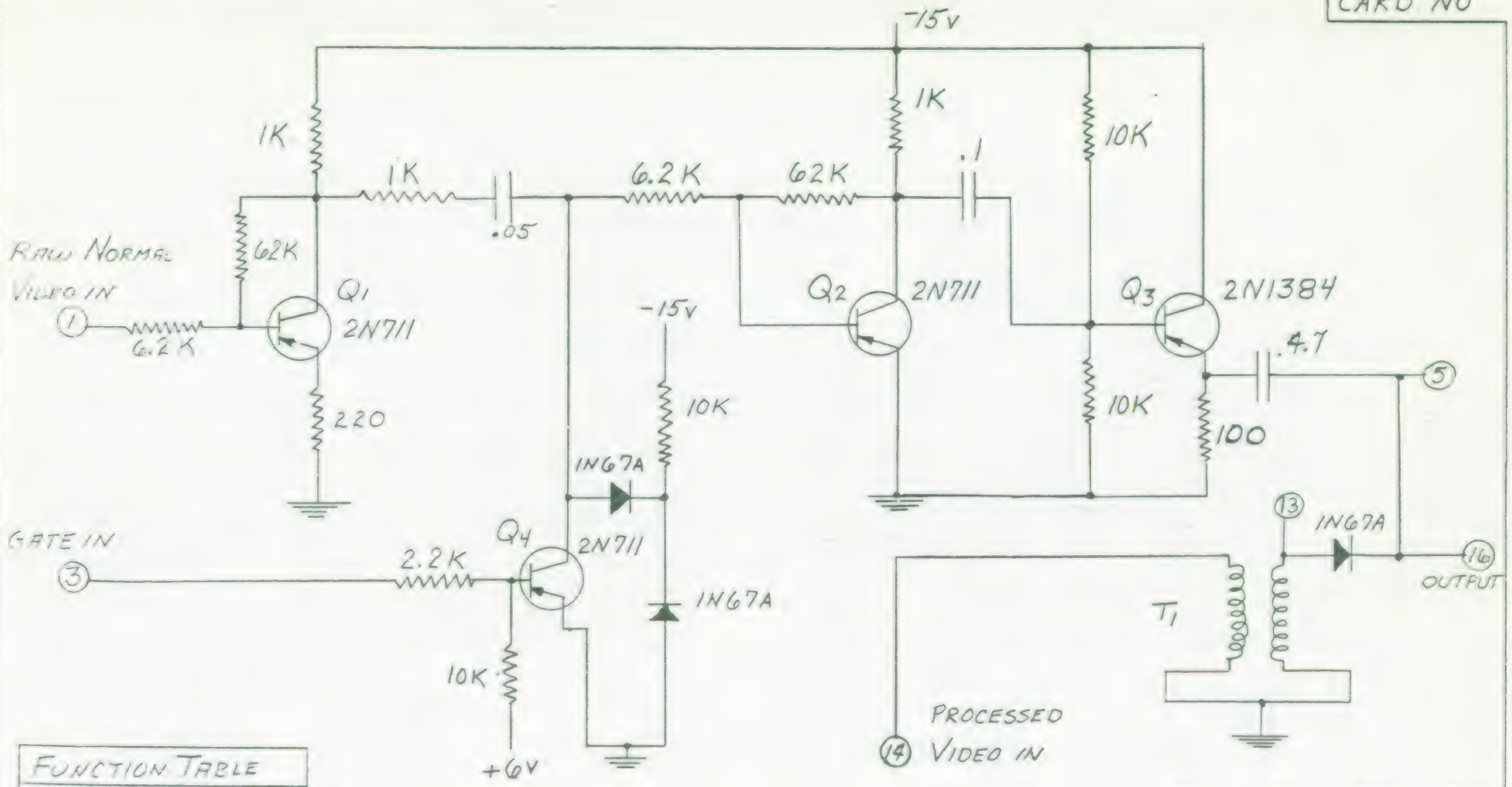
1. ALL CAP. IN μf
2. SEE TABLE FOR PIN CONNECTIONS
3. THIS CIRCUIT CONSTRUCTED ON A MATRIX CARD
4. F1 IS A UTC MQE 15; 2.8 HY. AT 7.2 ma.

FUNCTION TABLE	
PIN	FUNCTION
3	POS. TRIG OUTPUT
4	NEG. TRIG. OUTPUT
5	INPUT
6	GROUND
10	+6 V. DC
11	-6 V. DC
12	-15 V. DC
22	GROUND

FIGURE 33: TRIGGER AMPLIFIER, DATA PROCESSOR

CARD NO

1-23



FUNCTION TABLE	
PIN	FUNCTION
1	RAW NORMAL IN
3	NEG 6 MILE GATE
10	+6v
11	-6v
12	-15v
14	PROCESSED VIDEO IN
16	MIXED VIDEO OUT
22	GROUND

NOTES

1. ALL RESISTORS ½ WATT ±5% IN OHMS
2. ALL CAP. IN μf
3. TRANSFORMER T1 1:1 - 75 OHM OUTPUT TRANS.
4. THIS CIRCUIT IS BUILT ON A MATRIX CARD
5. SEE FUNCTION TABLE FOR PIN CONNECTIONS

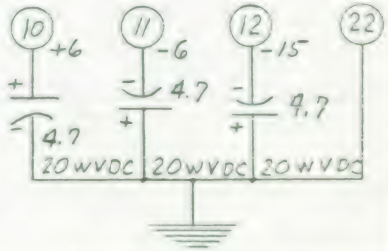
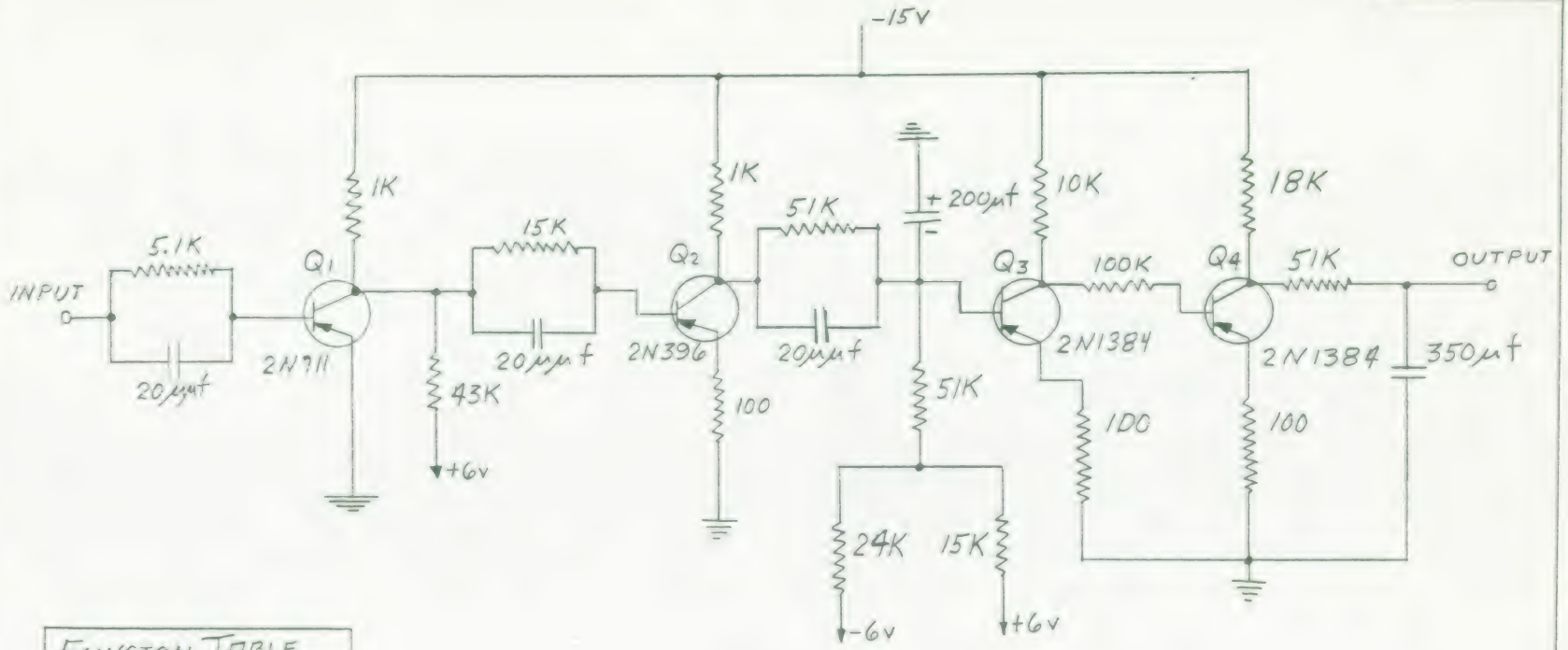


FIGURE 34:
VIDEO MIXER,
DATA PROCESSOR

CARD No.

1-3
1-6



FUNCTON TABLE	
PIN	FUNTION
4	OUTPUT
10	+6 V DC
11	-6 V DC
12	-15 V DC
16	INPUT
22	GROUND

NOTES

1. ALL RESISTORS ARE 1/2 WATT 5% IN OHMS
2. ALL CAP. IN μf UNLESS OTHERWISE SPECIFIED
3. SEE FUNCTION TABLE FOR PIN CONNECTIONS
4. 200μf CAP - SPRAGUE TE 1137 3/8" OD X 1 1/4 L
5. 350μf CAP - SPRAGUE 112 D 25/64" OD X 2 13/16"
6. 1 CIRCUIT PER CARD

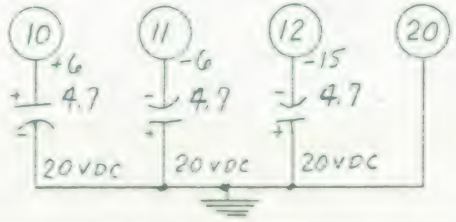


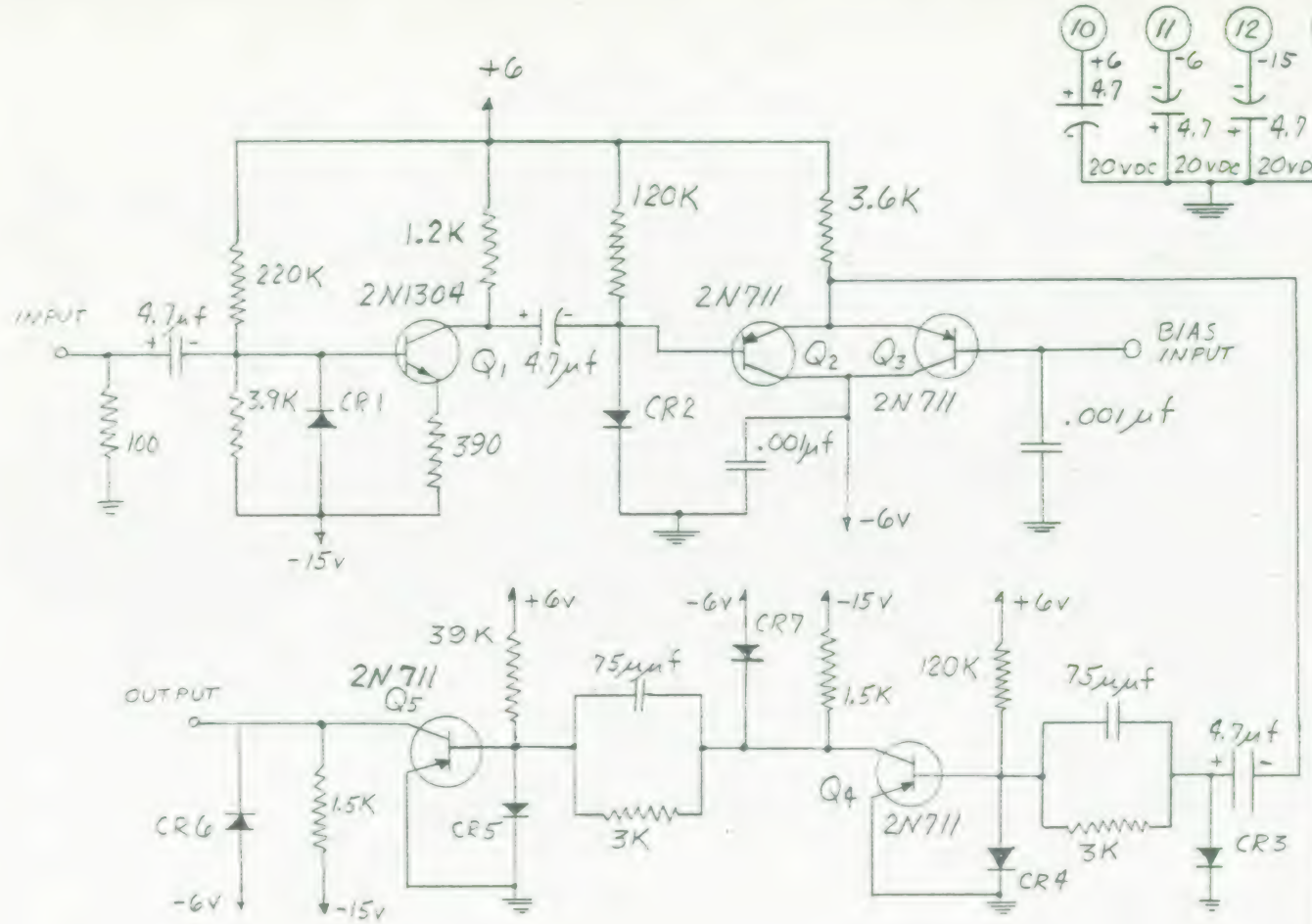
FIGURE 35:

AUTO CLIP LEVEL A,

DATA PROCESSOR

CARD No.

1-4
1-7



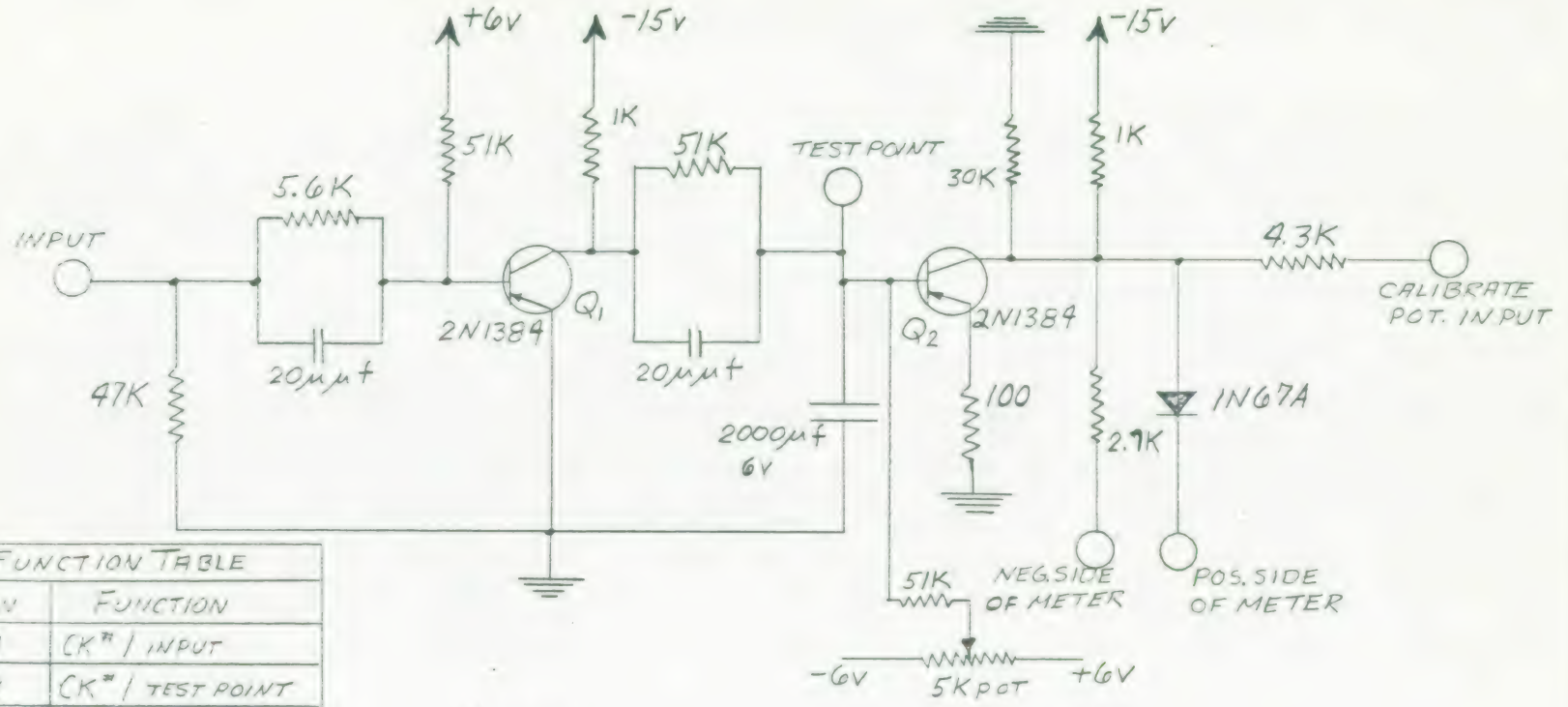
FUNCTION TABLE	
PIN	FUNCTION
4	OUTPUT
10	+6V
11	-6V
12	-15V
15	BIAS INPUT
17	INPUT
22	GROUND

NOTES

1. ALL RESISTORS 1/2 WATT 5%
2. ALL DIODES IN 67A
3. SEE FUNCTION TABLE FOR PIN CONNECTIONS
4. ALL CAP. IN μf UNLESS OTHERWISE SPECIFIED.

FIGURE 36:
AUTO CLIP LEVEL B,
DATA
PROCESSOR

CARD NO. 1-1



FUNCTION TABLE	
PIN	FUNCTION
1	CK#1 INPUT
2	CK#1 TEST POINT
4	CK#1 CALIBRATE POT INPUT
6	CK#1 NEG. SIDE METER
8	CK#1 POS. SIDE METER
10	+6V DC
11	-6V DC
12	-15V DC
15	CK#2 POS SIDE METER
17	CK#2 NEG. SIDE METER
19	CK#2 CALIBRATE POT. INPUT
20	CK#2 TEST POINT
21	CK#2 INPUT
22	GROUND

TO

NOTES

1. ALL RESISTORS ARE 1/2 W 5% IN OHMS
2. 2000μf CAP - SPRAGUE TVA-1106 $^{13}/_{16}$" O.D. × 2 $^{15}/_{16}$" L
3. THERE ARE TWO CIRCUITS PER CARD
4. SEE FUNCTION TABLE FOR PIN CONNECTIONS
5. 5K POT - BOURNS TRIMPOT 200L-1-502 5K 6101B

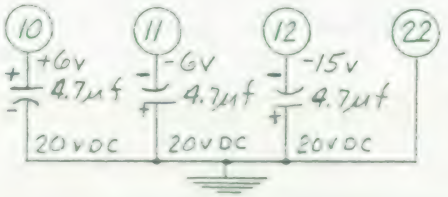


FIGURE 37:

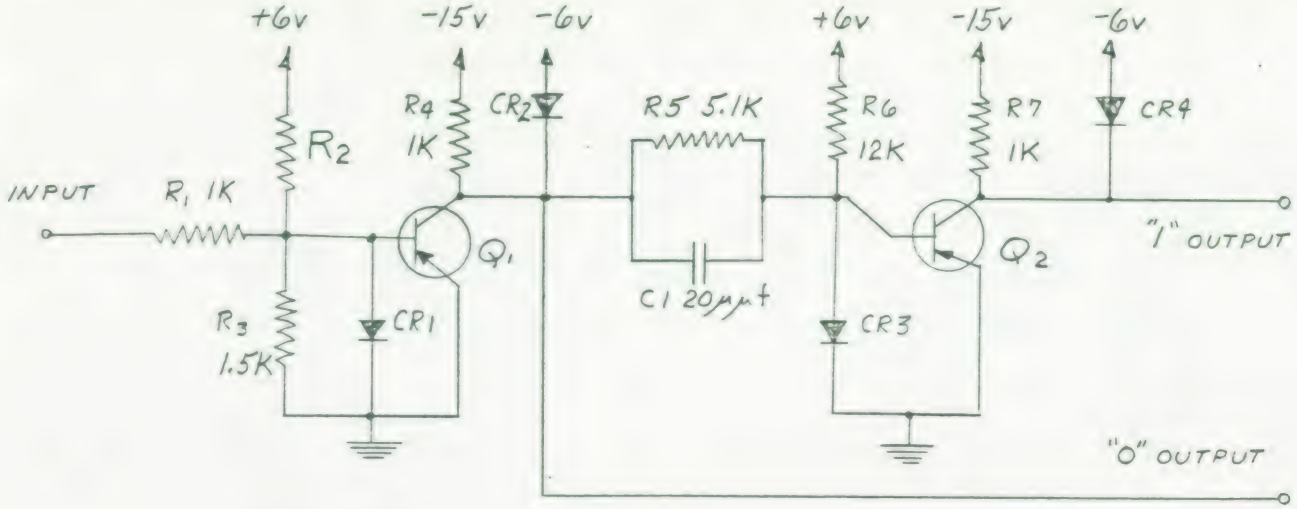
AUTO CLIP LEVEL C,

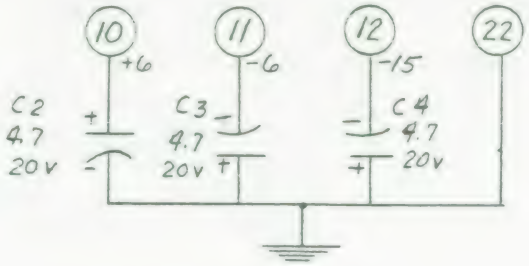
DATA PROCESSOR

CARD NO.

A1
7-4

A2
7-5





	SLICER A1 CARD			SLICER A2 CARD		
FUNCTION	CK#1	CK#2	CK#3	CK#1	CK#2	CK#3
INPUT	1	8	17	1	8	17
"1" OUTPUT	2	9	18	2	9	18
"0" OUTPUT	4	6	20	4	6	20
R_2	2.2K	2.7K	3.9K	4.7K	9.1K	47K

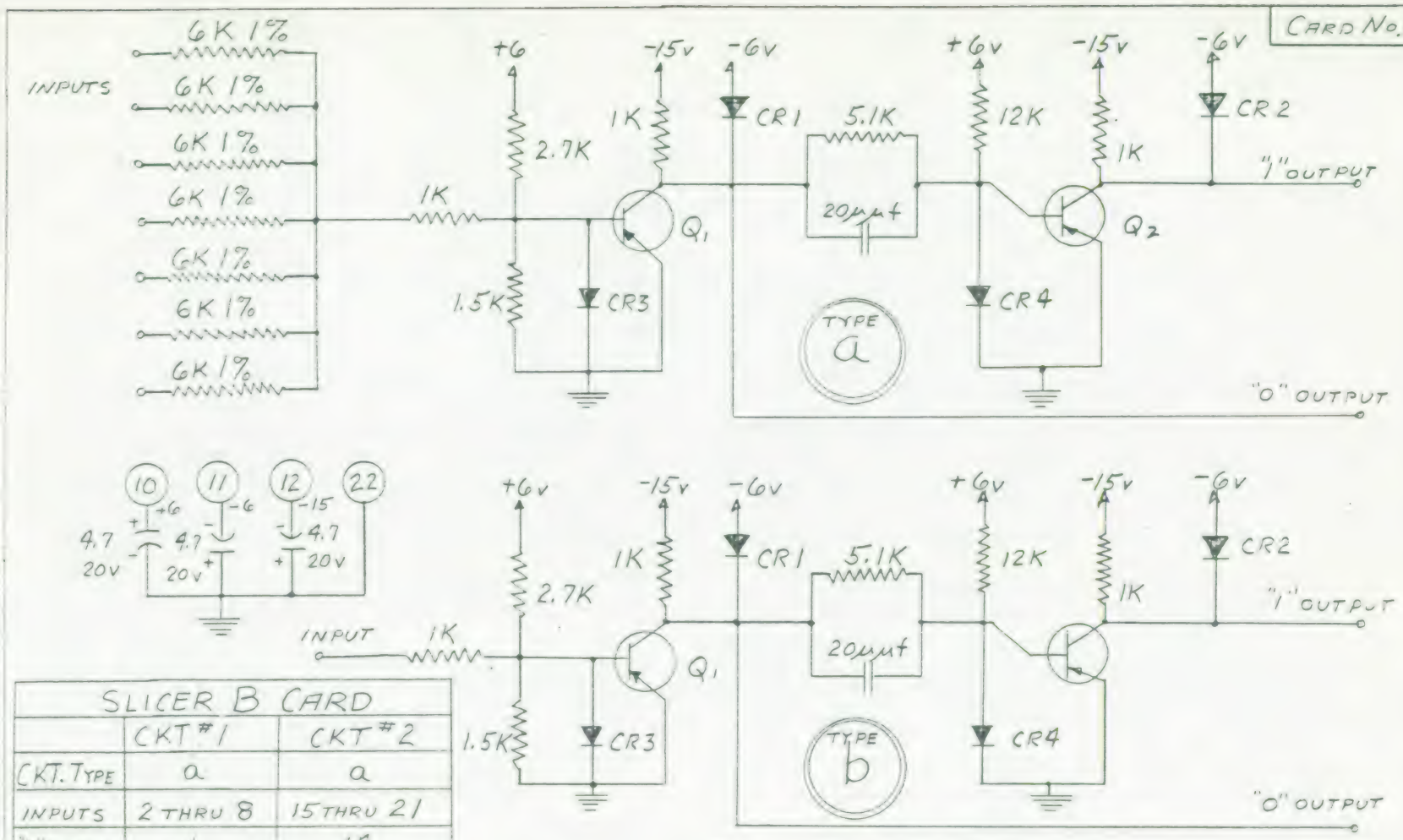
NOTES:

1. ALL RESISTORS ARE 1/2 WATT 5%
2. THERE ARE 3 CIRCUITS PER CARD
3. ALL TRANSISTORS ARE 2N711
4. ALL DIODES ARE IN67A
5. SEE TABLE FOR PIN CONNECTIONS
6. SEE TABLE FOR VALUES OF R2
7. BOTH CIRCUITS ARE BUILT ON SLICER A CARDS

FIGURE 38:

SLICER A1 AND A2,

DATA PROCESSOR



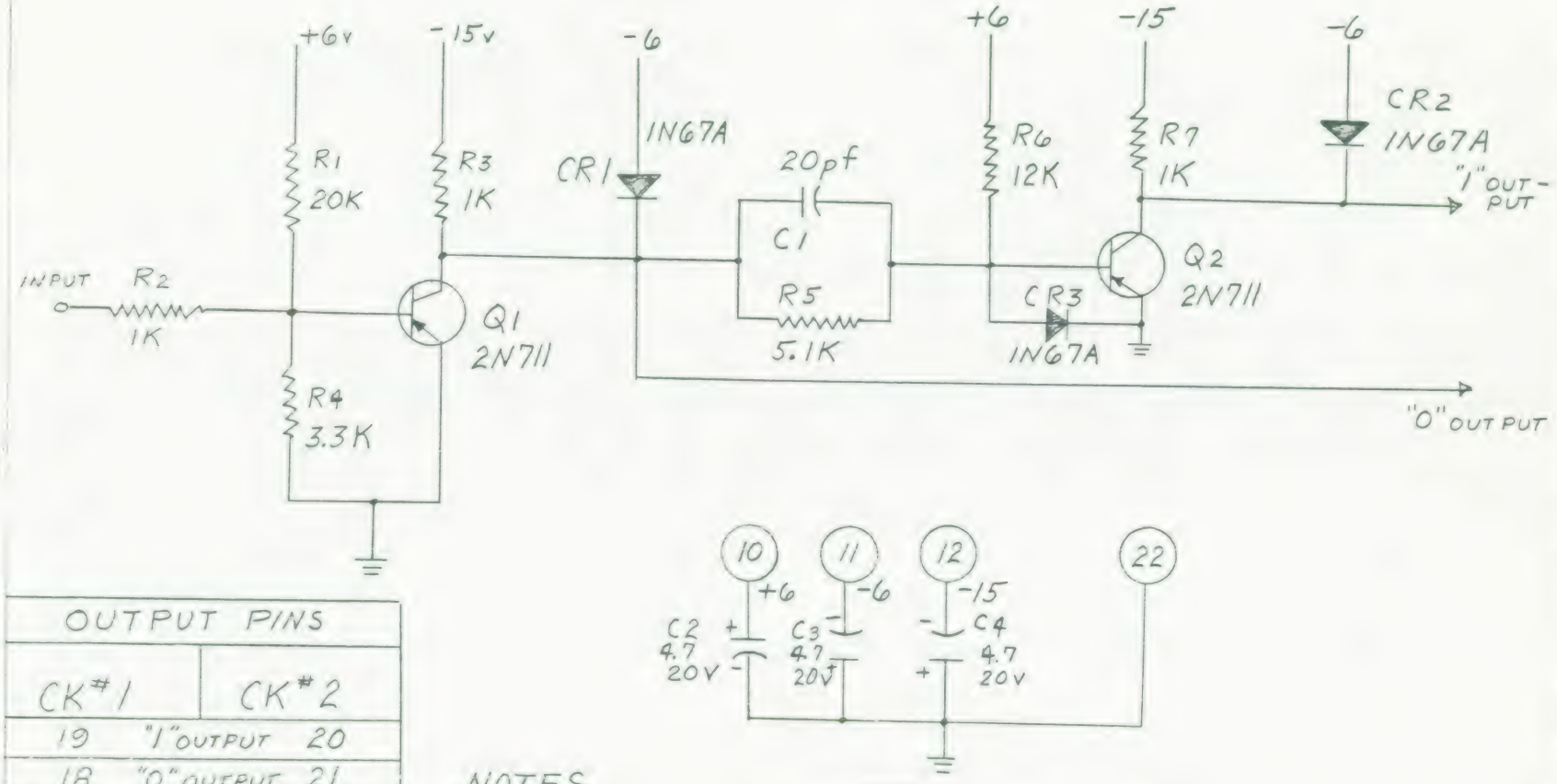
SLICER B CARD		
	CKT #1	CKT #2
CKT. TYPE	a	a
INPUTS	2 THRU 8	15 THRU 21
"1" OUTPUT	1	14
"0" OUTPUT	9	13

SLICER C CARD		
	CKT #1	CKT #2
CKT. TYPE	a	b
INPUTS	2 THRU 8	15
"1" OUTPUT	1	14
"0" OUTPUT	9	13

NOTES:

1. ALL TRANSISTORS ARE 2N711
2. ALL DIODES ARE 1N67A
3. ALL RESISTORS ARE 1/2 W 5% UNLESS OTHERWISE SPECIFIED
4. ALL CAP. ARE 1K W V DC IN μf
5. ALL CHROS HAVE 2 CIRCUITS OF THE TYPE SPECIFIED IN THE TABLES, BUILT ON SLICER BOARD
6. SEE TABLES FOR PIN CONNECTIONS

FIGURE 39: SLICER B AND C, DATA PROCESSOR



OUTPUT PINS	
CK#1	CK#2
19 "1" OUTPUT	20
18 "0" OUTPUT	21

NOTES

1. ALL RESISTORS ARE 1/2 W 5% SHOWN IN OHMS
2. UNLESS SPECIFIED ALL CAP. ARE GIVEN IN μf.
3. LOAD RES. FOR AND/OR CIRCUIT = 6.2K
4. TWO CIRCUITS PER CARD WITH VARIOUS COMBINATIONS OF INPUT CIRCUITS CLASSIFIED AS MATRIX A, B, C, D, E, F, AND G.

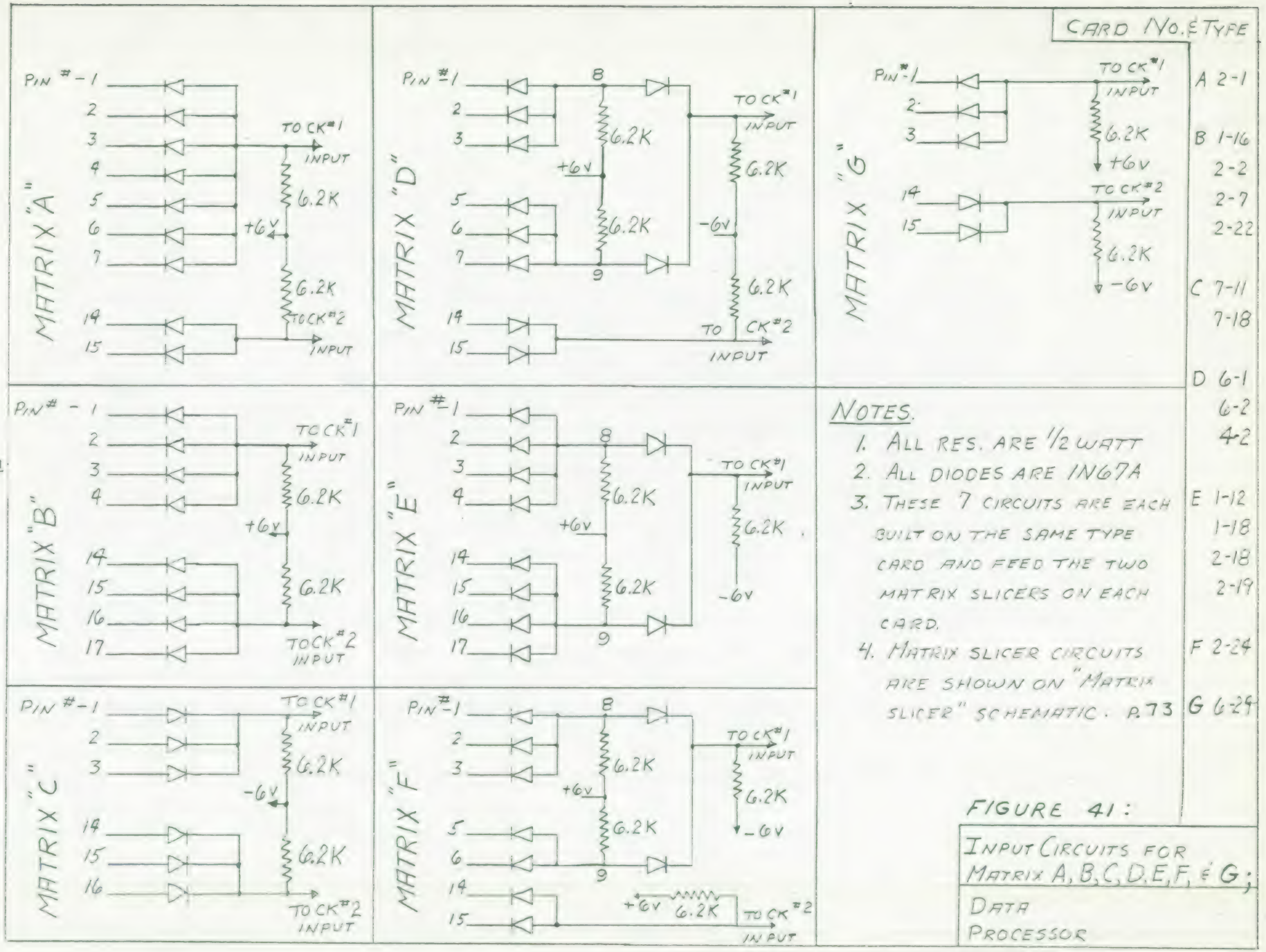
INPUT CIRCUITS ARE SHOWN ON "MATRIX INPUT" SCHEMATIC. P. 74

CARD No. & TYPE
A 2-1
B 1-16
2-2
2-7
2-22
C 7-11
7-18
D 6-1
6-2
4-2
E 1-12
1-18
2-18
2-19
F 2-24
G 6-24

FIGURE 40:

MATRIX SLICER FOR ALL MATRIX CARDS,

DATA PROCESSOR


MATRIX "A"
PIN # - 1
2
3
4
5
6
7
14
15
TO CK #1 INPUT
6.2K
+6V
6.2K
TO CK #2 INPUT
MATRIX "B"
PIN # - 1
2
3
4
14
15
16
17
TO CK #1 INPUT
6.2K
+6V
6.2K
TO CK #2 INPUT
MATRIX "C"
PIN # - 1
2
3
14
15
16
TO CK #1 INPUT
6.2K
-6V
6.2K
TO CK #2 INPUT
MATRIX "D"
PIN # 1
2
3
5
6
7
14
15
8
9
6.2K
+6V
6.2K
TO CK #1 INPUT
6.2K
-6V
6.2K
TO CK #2 INPUT
MATRIX "E"
PIN # 1
2
3
4
14
15
16
17
8
9
6.2K
+6V
6.2K
TO CK #1 INPUT
6.2K
-6V
MATRIX "F"
PIN # 1
2
3
5
6
14
15
8
9
6.2K
+6V
6.2K
TO CK #1 INPUT
6.2K
-6V
+6V 6.2K
TO CK #2 INPUT
MATRIX "G"
PIN # 1
2
3
14
15
TO CK #1 INPUT
6.2K
+6V
TO CK #2 INPUT
6.2K
-6V
CARD NO. & TYPE
A 2-1
B 1-16
2-2
2-7
2-22
C 7-11
7-18
D 6-1
6-2
4-2
E 1-12
1-18
2-18
2-19
F 2-24
G 6-29
NOTES.
1. ALL RES. ARE 1/2 WATT
2. ALL DIODES ARE IN67A
3. THESE 7 CIRCUITS ARE EACH BUILT ON THE SAME TYPE CARD AND FEED THE TWO MATRIX SLICERS ON EACH CARD.
4. MATRIX SLICER CIRCUITS ARE SHOWN ON "MATRIX SLICER" SCHEMATIC. P. 73
FIGURE 41:
INPUT CIRCUITS FOR MATRIX A, B, C, D, E, F, & G;
DATA PROCESSOR

This same problem was eliminated at the summation of the memory outputs with an emitter follower. Emitter followers were installed on all slicer B and C cards.

The following problems which occurred have not yet had satisfactory explanations and/or have not been corrected.

1. There are no fine range targets at the output when the test pattern is applied and the unit is in the high resolution mode.
2. The Processor is designed to compensate for two miles of delay but it appears that the unit has almost three miles of delay. The Rescon personnel felt this extra delay was due to an accumulation of many small delays. This could easily be compensated for by the addition of two flip-flop circuits clocked with the appropriate pulses.
3. A clip lead from 1-8-14 to 1-14-7 was left in the equipment. This is the output of Q2 prime side fed to the prime side "and" input of Q4. Rescon felt this had to be done to permit proper action in Q4 when the test pattern was applied.

None of these problems affected the study undertaken in this report, and so were not investigated.

The machine contains a total of 168 cards as follows:

CARD NAME	QUANTITY	CARD NAME	QUANTITY
1. ACL-A	2	12. Matrix B	4
2. ACL-B	2	13. Matrix C	2
3. ACL-C	1	14. Matrix D	3
4. FFB	101	15. Matrix E	4
5. FFA	27	16. Matrix F	1
6. Slicer A1	1	17. Matrix G	1
7. Slicer A2	1	18. Video Mixer	1
8. Slicer B	1	19. Trigger Amp	1
9. Slicer C	1	20. Adder	1
10. Clock Driver	11	21. Clock Oscillator	1
11. Matrix A	1		

It should be noted that some of the circuits occurring only once in the machine are built on one of the more frequently used cards. When this was done, some modifications on the card had been performed. This can most easily be detected by looking at the modified cards listed below:

1. The Trigger Amplifier (4-1) is built on a standard matrix card.
2. The ACL-C (1-1) has been modified with the addition of two 5K trimmer potentiometers.
3. The Video Mixer (1-23) is built on a standard Matrix card.
4. The Adder and Emitter Follower (7-3) are built on a slicer B card.
5. Slicers A1, A2, B, and C had to have additional leads brought out to pins so as to supply the prime output to their respective serial shift registers. The reason for this was described on Page 75, Paragraphs 4 and 5.

For the convenience of wiring, all cards use the same pins for power supply voltages.

+6 volts	Pin 10
-6 volts	Pin 11
-15 volts	Pin 12
Ground	Pin 22

The power supply is regulated D.C. supply furnished by Dynamic Controls Corporation of Cambridge, Massachusetts. Voltage supplied by it are +6 volts at 5 amps, -6 volts at 5 amps, and -15 volts at 10 amps.

The magnetic core memory utilized in the data processing equipment was supplied by General Ceramics, Division of Indiana General Corporation. The unit is a Buffer Memory Model 128K32CF, capable of storing 32 bits of information in each of 128 registers. Their plant is located in Keasbey, New Jersey.

E X P A N D E D T H E O R Y O F O P E R A T I O N

The following is an expanded theory of operation for Paragraphs 3.3 and 3.4 in the Rescon Final Report on the Video Digital Processor.

3.3 Sliding Window Detector and Video Integrator: The data from either the high resolution registers or from Q6 and FN is applied to the input of Memory Bit #1. This dats is stored in the appropriate memory range register for the remainder of that radar trigger interval. The information in each of the 128 registers represents one range interval. The information in each range interval for the previous 16 range sweeps is sampled at the memory output by a resistive

adder and six target detection slicers. Information as to whether there are four, six, eight, ten, twelve, or fourteen hits out of any sixteen consecutive triggers during any range interval is then available at the output of the appropriate slicer. This integrated and detected information, representing a sampling of data with respect to azimuth density, is now applied to the automatic mapper and output section.

3.4 Automatic Mapper: The actual details of automatic mapping can be supplemented by the use of logic equations. After the information is sampled by the slicers it is shifted into the appropriate D channel register which stores it for a given number of consecutive range intervals. The D4, D6, and D8 registers are sampled by resistive adders coupled to target detection slicers AMD4, AMD6, and AMD8 which detect 3 hits out of 7 consecutive range intervals. This enables range density information to be sampled along with the azimuth density sampled in the previous slicers. See Figure 29, Page 60. These slicers feed three stage shift registers D4B, D6B, and D8B which store range sampling information for application to matrices G4, G6 and G8.

Using Matrix logic equations:

1. $(D4B1 + D4B2 + D4B3) = G4$

This equation states that if the automatic map criteria was met for any of the three previous consecutive groups of seven range increments, a pulse from D4B1, D4B2, or D4B3 will be fed to $\widetilde{G4}$ and to the input of memory bit 17.

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2. $(M17 + G4) = \widetilde{G4'}$

When an output from G4 or data from a previous radar trigger period is fed into G4', the output will be a -6 volt pulse. This will prevent an output from A1 which, in effect, cancels that particular target.

3. $\widetilde{G4'}\ (B'D6 + B\ D4) = A1$

a) For $\widetilde{G4'}$ at ground (from equation 2) and B' at ground due to no target in that range interval during the previous radar trigger period, D6 criteria will then establish the presence of a target. This will permit a target out of A1.

b) For $\widetilde{G4'}$ at ground (from equation 2) and B at ground indicating a target in that range interval during the previous radar trigger period, D4 criteria will be sufficient for the continuing presence of a target. This also will permit a target out of A1.

The above explanations likewise apply to the following equations leading to a target out of A2 or A3.

$$M18 + (D6B1 + D6B2 + D6B3) = \widetilde{G6'}$$

$$M19 + (D8B1 + D8B2 + D8B3) = \widetilde{G8'}$$

and

$$\widetilde{G6'}\ (B'D10 + BD8) = A2$$

$$\widetilde{G8'}\ (B'D14 + BD12) = A3$$

4. $(A1 + A2 + A3) = \widetilde{A}$

An output from any one of the three (A1, A2 or A3) will establish an output from $\widetilde{A}$. This is fed to the input of memory bit 20 so the unit will be aware that a target occurred during the previous sweep within the range interval. The output from $\widetilde{A}$ is also applied to $\widetilde{D}$ along with

fine range information so that a target will be placed in the proper half of the corresponding range interval. This is shown in equation 5.

5. $(\widetilde{RN2}\ \widetilde{A}\ \widetilde{FR'} + \widetilde{A}\ \widetilde{FR}\ \widetilde{RN1}) = \widetilde{d}$

Since $\widetilde{d}$ is now the processed data ready for application to the PPI, it remains only to mix this data with the raw video occurring beyond the data processor range. This is accomplished in the video mixer circuit $\widetilde{dt}$.

A P P E N D I X II

PROCESSOR CIRCUIT CHANGES

A P P E N D I X II

The following is a list of the changes which were made to the processor in order to incorporate the additional circuitry necessary to produce the digital STC waveform. To return the processor to its original conditions, reverse the procedure. The numbers used represent Pin locations as shown below.

2	15	6
Rack Location Numbered from top	Card Location Within Rack Numbered from left	Pin Location on card, numbered from top

Rack number 8 is the added STC circuitry.

1. Original lead to 1-19-4, 5 lifted, yellow wire from 8-1-20 connected to lifted lead.
2. Original lead to 1-15-7 lifted and taped, pin 1-15-7 now fed by brown wire from 8-2-18.
3. Original lead to 1-15-2 lifted and connected to lead lifted from 1-12-19.
4. Pin 1-15-2 now fed by green wire from 8-2-19.
5. Original lead to 1-14-2 lifted and taped.
6. Pin 1-14-2 now fed by white/purple wire from 1-12-19.

7. Blue wire from 8-23-18 connected to 2-8-18.
8. White wire from 8-23-21 connected to 2-24-18.
9. Violet wire from 8-23-1 connected to 7-24-3.
10. Original lead to 6-23-17 lifted and taped.
11. Brown/white wire from 8-2-2 connected to 6-23-17.
12. Original lead to 4-23-17 lifted and taped.
13. Yellow wire from 8-2-1 connected to 4-23-17.
14. Brown wire from 8-22-18 connected to 1-2-17.
15. Original lead to 2-8-5 lifted, lifted lead reconnected to 2-8-16.
16. Original lead to 1-18-1, 2 lifted and taped.
17. New lead installed from 2-8-5 to 1-18-1, 2.
18. Original lead to 1-13-17 lifted and taped.
19. New lead installed from 1-13-17 to 2-13-8.
20. New lead installed from 1-13-4 to 2-13-1.

B I B L I O G R A P H Y

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13. ABSTRACT

The need for improved Sensitivity Time Control circuits in Air Traffic Control radar equipment becomes more imperative as Emergency Mission System search and precision radars become more sensitive and all-weather tracking and controlling to within a mile of the radar site becomes standard procedure. This report traces the development of a sophisticated logarithmic STC circuit from previously derived concepts through incorporation in, and evaluation of, the latest EMS search radar. The development of Digital Video Data processing equipment led to design and experimental work on a digital STC concept. The preliminary investigation of this concept indicates that a significant advance in this direction is possible in clutter attenuating devices. Reference is also made to the current EMS system including test results plus recommendations for improvements in anti-clutter devices for present and future search and precision radars.

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